JNEye User Guide

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2015.05.04

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System Requirements and Installation Guide

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JNEye is a high-speed transceiver link simulation. When you design high-speed, multi-gigabit transceiver links, you must ensure the end-to-end performance from transmitter (TX) to receiver (RX) and all interconnects in between.

JNEye's graphical user interface (GUI) and link simulator allow you to quickly and easily set up and evaluate high-speed link performance early in your design cycle. JNEye also helps you identify possible issues in board level design. With JNEye, you can quickly estimate optimal link equalization and other electrical parameter settings for transmitter and receiver. You can also use JNEye to predict link performance such as jitter and noise at a small probability level.

System Requirements

JNEye has the following minimum system requirements:

- Microsoft Windows XP, Windows 7, or Windows 8
- 4 GB RAM
- 3 GB storage space
- Microsoft .NET Framework 4

JNEye requires a Quartus® II software subscription license to perform simulations, design channels, and view channel characteristics. Contact your Altera sales representative or your system administrator if you have questions regarding accessing the Quartus II software subscription license.

Related Information

- **Download Microsoft .NET Framework 4**
- **Download Microsoft Visual C++ 2013 Library**

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Installation

To install JNEye, perform the following steps:

1. Acquire the **JNEye 15.0 Installation Package** from the Altera Download Center.
2. Execute the installation file to install JNEye.
   a. To improve the performance of the JNEye 64-bit version, the JNEye Installer asks for administration-level access right to install additional Microsoft .NET components.
   b. If the installer cannot get administration-level access, the installation installs both 32-bit and 64-bit JNEye components. You can install the additional .NET components after installation when you can grant administration-level access to your computer.
   c. If the installer can acquire the administration-level access (given user approval/acknowledge), the installer automatically includes and installs the additional .NET components. The installation process is much longer (can exceed 10 minutes) than previous JNEye releases.
3. Execute **JNEye.exe** to start JNEye. The JNEye 15.0 release comes with both 32-bit and 64-bit executables. 32-bit JNEye is located in <*JNEye Installation Directory*>**\bin** and 64-bit JNEye is in <*JNEye Installation Directory*>**\bin64**.

JNEye requires an Altera Quartus II Subscription License to perform simulations and view channel characteristics. Contact your Altera sales/supports or your system administrator if you have questions about obtaining an Altera Quartus II Subscription License.

JNEye automatically checks the license server specified in the system environment variable "LM_LICENSE_FILE" for the required license. The license checking configuration can be configured by editing the following entries in the configuration file **JNEye_Config.dat**:

- **%% LM_License_File_Name**—License file name. If a license server is used, this entry is ignored. The default value is **na**. JNEye automatically checks whether a license server exists. If a valid license server does not exist, JNEye checks the individual license file specified in this entry.
- **%% LM_License_Feature_Name**—The feature or type of license to be checked out for JNEye use. The default value is **quartus**.

When you execute JNEye for the first time, JNEye may ask permission to create a JNEye working directory at <*JNEye Installation Directory*>**\GUI_Work**.

Click **Yes** to use the default location. To use a different working directory, modify the "%% GUIWorkDirectory" entry in **JNEye_Config.dat**.

If you have problems running JNEye after installing the program, follow these instructions:

- **Check whether the Microsoft Visual C++ 2013 library is on your system**
  - If you execute JNEye in a system that doesn't have the Microsoft Visual C++ 2013 library, you will get an error message.
  - Download the Visual C++ 2013 library from the Microsoft web site and install it.

    Note: For 64-bit Windows operating systems, the 32-bit version of the Visual C++ 2013 library is required for running the 32-bit version JNEye.
- **Check whether Microsoft .NET Framework 4 is on your system**
  - If you execute JNEye Release in a system that doesn't have Microsoft .NET Framework 4, you will get an error message.
  - Download .NET Framework 4.0 from the Microsoft web site and install it.
    - 32-bit Windows: Execute **dotNetFx40_Client_x86.exe**
    - 64-bit Windows: Execute **dotNetFx40_Full_x86_x64.exe**
  - You may have to install Windows Imaging Component (WIC) before installing .NET Framework 4. You can download WIC from the Microsoft web site.

Related Information

Download Windows Imaging Component

Program and File Types

JNEye comes with the following executable files:

- **JNEye.exe**—JNEye's main user interface
- **JNEye_Simulation_Engine.exe**—JNEye simulation engine
- **JNEye_Simulation_Engine_Console.exe**—JNEye simulation engine (console version)
- **JNEye_Data_Viewer.exe**—The JNEye Data Viewer displays simulation results
- **JNEye_Channel_Viewer_SA.exe**—The JNEye Channel Viewer displays channel characteristics
- **JNEye_Batch_Simulation_Controller.exe**—The JNEye Batch Simulation Controller runs simulations in batch mode
- **JNEye_Channel_Designer.exe**—JNEye's channel designer that generate S-parameter channel models for link simulations

JNEye uses the following file extensions:

- **.jne**—JNEye simulation configuration
- **.jneschm**—JNEye simulation schematic configuration
- **.jnetxdata**, **.jnerxdata**, **.jnedevdata**, **.jneledata**, and others—JNEye internal data

When you want to share a JNEye link configuration, both **.jne** and **.jneschm** files are needed for other users to reload the link configuration in his or her JNEye session. Make sure all other associated files, such as channel model files and device model files, are included so that simulations can be run correctly. JNEye provides limited backward compatibility with link configuration files saved in previous versions.

Functional Description 2

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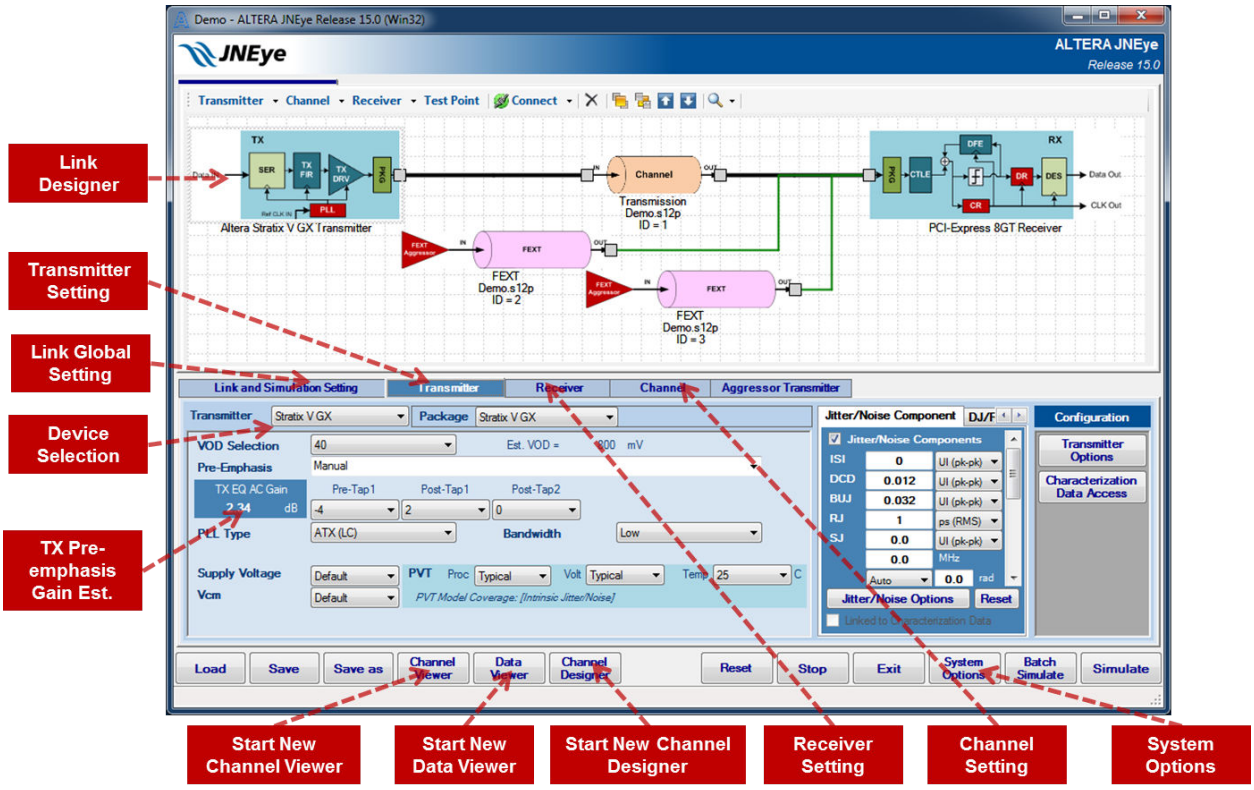
JNEye Control Module

Double-click the **JNEye.exe** icon to launch JNEye.

Figure 2-1: JNEye Control Module



Constructing Communication Links in the Link Designer Module

The Link Designer module allows you to construct communication links.

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Figure 2-2: JNEye Link Designer Module

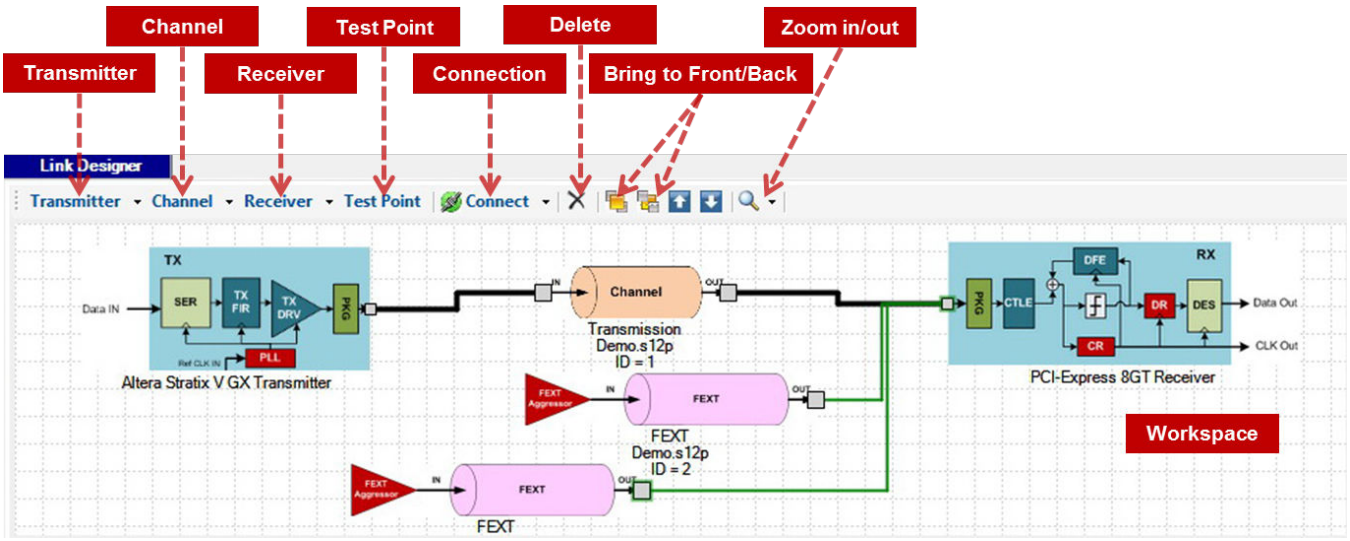


Table 2-1: Supported Transmitter, Channel, and Receiver Components

Transmitter (TX) Component	Channel Component	Receiver (RX) Component
Altera Stratix V GX	Transmission	Altera Stratix V GX
Altera Arria V GZ	Connector	Altera Arria V GZ
Altera Stratix V GT	Far-end Crosstalk	Altera Stratix V GT
Altera Arria 10 GX/SX	Near-end Crosstalk	Altera Arria 10 GX/SX
Altera Arria 10 GT	Package	Altera Arria 10 GT
IBIS-AMI	AC Coupling Capacitor	IBIS-AMI
Custom	Shunt Capacitor	Custom
PCI-Express 8GT		PCI-Express 8GT

JNEye supports the following simulations:

- Altera TX to Altera RX
- Altera TX to non-Altera RX
- Non-Altera TX to Altera RX

Note: Non-Altera to non-Altera link simulations are not supported.

A link consists of a transmitter, a receiver, and one or more channel components. Select the transmitter, receiver, and channel components from the menus at the top of the Link Designer workspace.

After the link components are placed into the workspace, click **Connect** to connect the components. In connect mode, one or two connectors are shown on each component. Connect the link components by dragging the line from one connector to another. Two types of connections are provided in Link Designer: **Right Angled Line** and **Straight Line**. Right Angled Line is the default connection method. Test

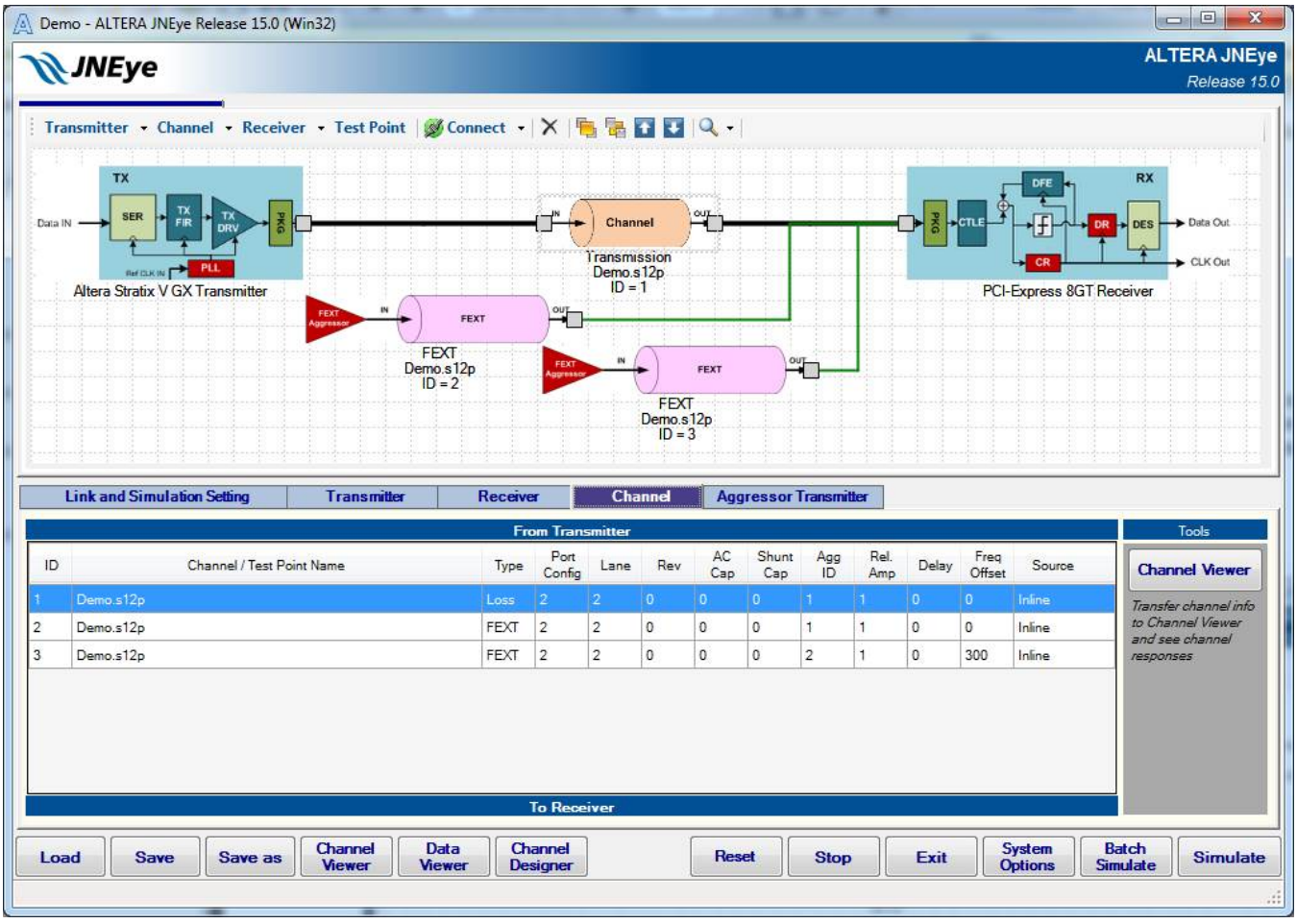
points can be manually placed into the link by clicking **Test Point** and connecting to the desired location in the link.

The following rules of link construction apply to the Link Designer module:

- A transmitter can only have one output port or connector
- A receiver can only have one input port or connector
- A channel component has one input and one output port
- A test point can only be connected to an input port
- A connection between two components can be established from an output port to an input port
- A transmitter cannot be connected directly to a receiver

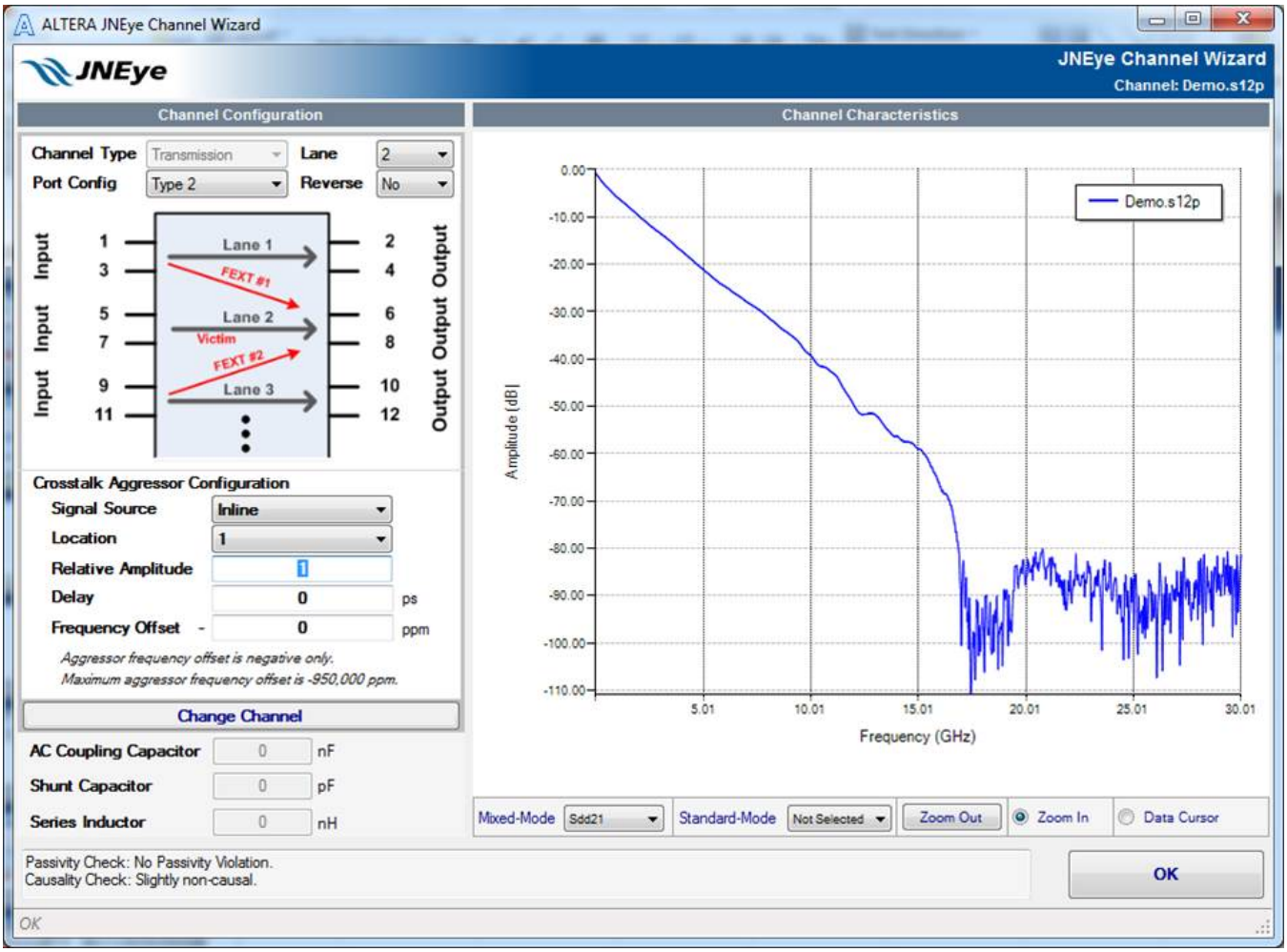
A link establishment checking algorithm runs constantly in the background, checking whether a link is established for simulations. When a link is established between a transmitter and receiver, the link lines become bold and color-coded. Bold black lines indicate signal paths, green lines indicate crosstalk signal paths, and purple lines point to test point port locations. The following figure shows an example link topology. A table of link components is displayed in the Channel tab for reference.

Figure 2-3: JNEye Link Designer with Channel Table



When a channel component (for example, a transmission line, connector, far-end crosstalk (FEXT), near-end crosstalk (NEXT), package, AC coupling capacitor, or shunt capacitor) is chosen, the **Channel Wizard** helps you verify or set the channel configuration.

Figure 2-4: JNEye Channel Wizard



The Channel Wizard displays the channel characteristics and allows you to verify the correctness of the channel component, such as a component represented by an S-parameter. The Channel Wizard allows you to select a channel type, port configuration, signal lanes (for multiple-lane S-parameters with eight and more ports), crosstalk aggressor location (for multiple-lane S-parameters), aggressor, series inductance value (in nH), AC coupling capacitor value (in nF), and shunt capacitance value (in pF). The Channel Wizard checks the integrity of the channel component in terms of passivity and causality characteristics. When the Channel Wizard detects passivity and causality violations, it displays messages about the severeness of the violations in the text box on the left of the **OK** button. The levels of channel integrity violation are listed in the following tables.

Table 2-2: Channel Passivity Check Results and Recommendations

Passivity Violation Check Results	Impact on Link Simulation Accuracy	Recommendations
No Passivity Violation	No impact	No action needed

Passivity Violation Check Results	Impact on Link Simulation Accuracy	Recommendations
Slight Passivity Violation	There may not be a noticeable effect in the simulation result	The channel model can be further improved but the improvement in terms of simulation results accuracy can be small.
Minor Passivity Violation	There may be a noticeable effect in the simulation result	The channel model can be further improved. The differences in terms of simulation results and accuracy are expected.
Passivity Violation	Simulation result will be impacted	The channel model needs to be regenerated (by design tools) or re-taken (by instruments). The confidence of simulation results using this channel model is low.

Table 2-3: Channel Causality Check Results and Recommendations

Causality Violation Check Results	Impact on Link Simulation Accuracy	Recommendations
Channel is causal	No impact	No action needed
Slight non-causal	There may not be a noticeable effect in the simulation result	The channel model can be further improved but the improvement in terms of simulation results accuracy can be small.
Somewhat non-causal	There may be a noticeable effect in the simulation result	The channel model can be further improved. The differences in terms of simulation results and accuracy are expected.
Non-causal	Simulation result will be impacted	The channel model needs to be regenerated (by design tools) or re-taken (by instruments). The confidence of simulation results using this channel model is low.

To select another S-parameter within the Channel Wizard, click **Change Channel**.

Note: Altera recommends that you replace or change a channel with one of the same channel type. Link Designer allows channel changing with different channel types, but you might see inconsistent channel icons in the design workspace.

An existing channel can be changed by adding a new channel component or by modifying an existing channel component. Right-click in the Link designer module and select **Properties**.

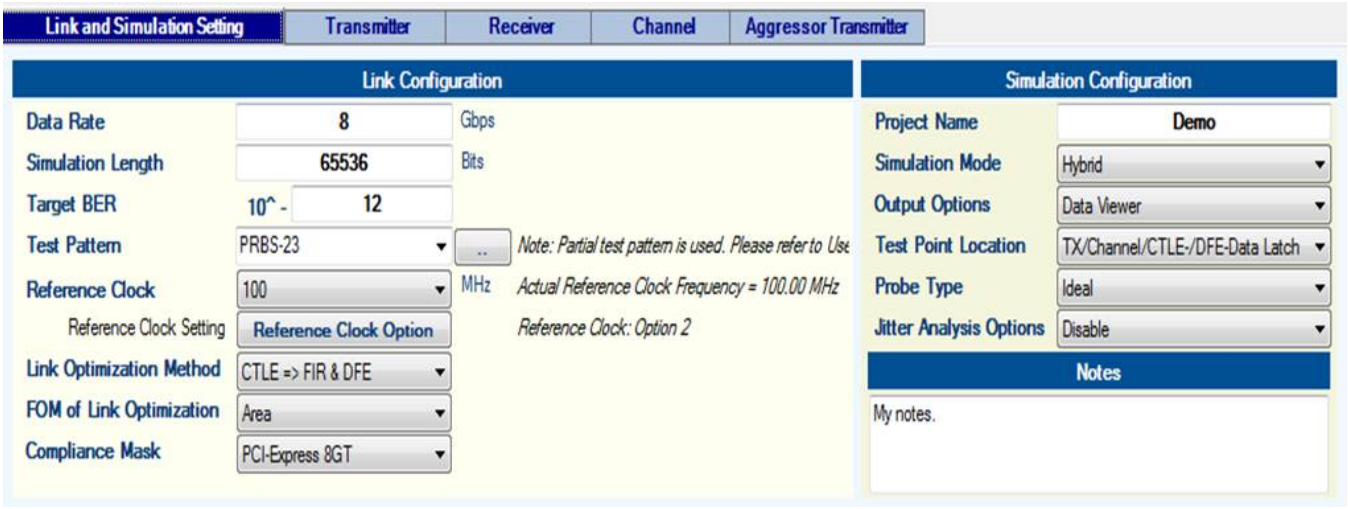
When using the package channel component, follow these guidelines:

- Package models should be placed next to the devices.
- Each device can have only one package model. Therefore, the external package model can only be used when the device's package type is "Custom".
- The package model type is used by the simulation engine to identify the boundary of the devices and generate a waveform for observation and analysis.
- The package model is treated the same way as the "Transmission" channel type. Therefore, use the "Transmission" channel type even if the model represents a physical package (in your system) but it is not a package of the TX and RX.

Link and Simulation Setting

The **Link and Simulation Setting** tab sets the global link parameters and simulation configurations.

Figure 2-5: Link and Simulation Setting Tab



The **Link and Simulation Setting** dialog box contains the following fields.

Data Rate

Link data rate is specified in Gbps.

Simulation Length

Simulation length is specified in the number of bits running at the specified data rate. Simulation length should be at least 4096 bits. Altera recommends that the length is a power-of-2 factor for the best computation efficiency. The simulation length does not apply in Statistical mode.

Note: Simulation length is adjusted automatically to the closest power-of-2 factor.

Target BER

Target bit error rate is used to calculate the jitter and noise at low BER conditions. The methodology of jitter and noise at low BER can be found in *HST Jitter and BER Estimator Tool User Guide for Stratix IV GT and GX Devices*.

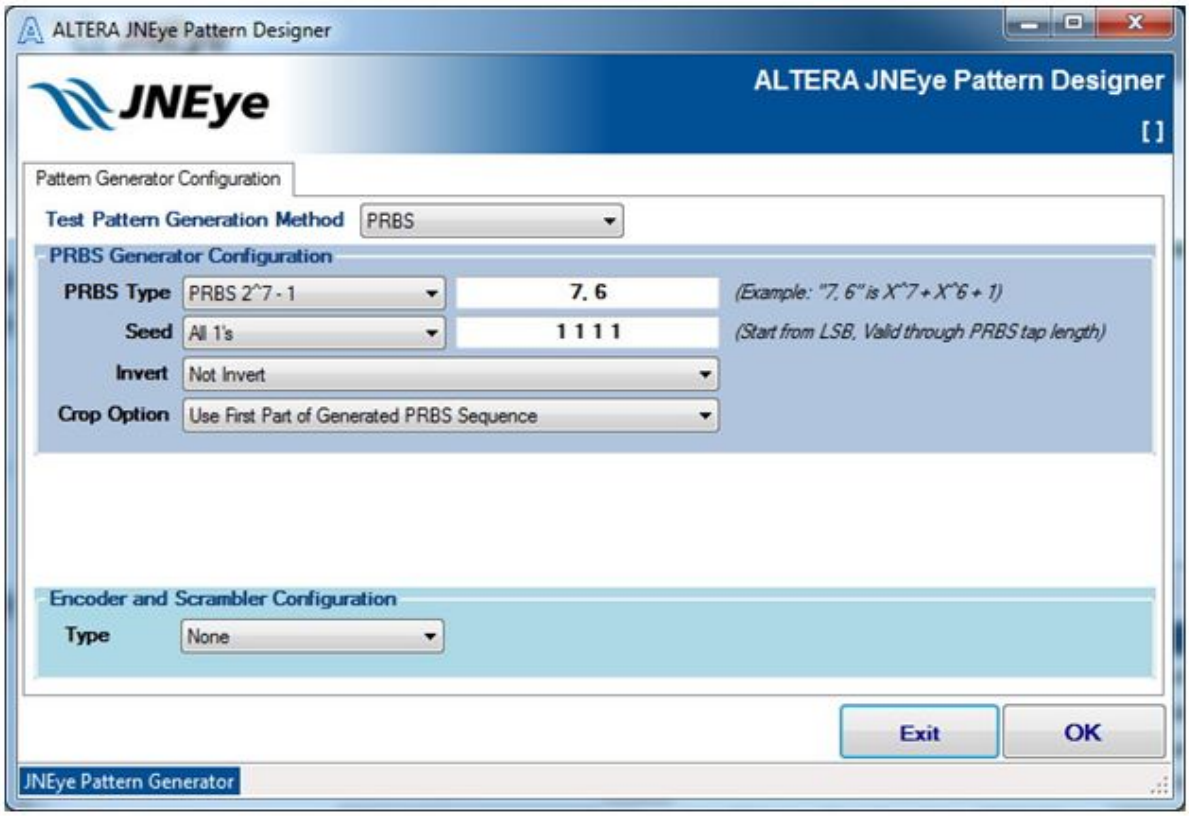
Test Pattern

Allows you to specify the test pattern used in the simulation. The following test patterns are available:

- **PRBS-7**, **PRBS-9**, **PRBS-11**, **PRBS-15**, **PRBS-23**, and **PRBS-31**
  - The PRBS test patterns are generated using JNEye's built-in pattern generator.
  - If the whole PRBS pattern is shorter than the simulation length, the PRBS pattern is inverted and repeated. The inversion is applied to achieve DC balance of the generated PRBS test pattern.
  - If the PRBS patterns are longer than the simulation length, a partial test pattern of the PRBS pattern is used. The default initial condition of PRBS test pattern generation is with logic 1s in all shift registers for the valid PRBS patterns.
  - The most commonly used PRBS test patterns are listed in the Test Pattern menu. Other PRBS test pattern can be selected or configured in the Pattern Designer.

- **Pattern Designer**—Allows you to specify your own custom test patterns. The following figure shows the Pattern Designer user interface.

Figure 2-6: JNEye Pattern Designer

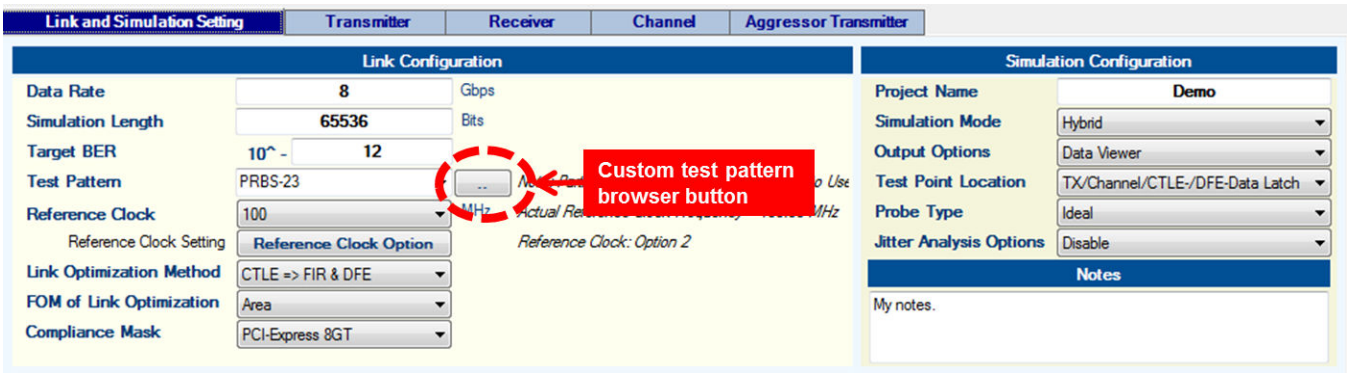


The Pattern Designer includes the following test pattern generation methods:

- **PRBS**—Provides an extensive list of common PRBS test patterns. You can also specify custom PRBS polynomials and seeds. The internal linear feedback shift register (LFSR) engine uses the information to generate the desired test pattern. Other options include selecting how the test pattern is repeated or extracted when the simulation length is longer or shorter than the generated test patterns. There are two options for selecting the partial test patterns:
  - **Use First Part of Generated PRBS Sequence**
  - **Include Longest Run-Length Bit Sequence**—The longest run-length test pattern will be located at the ending portion of the test bit sequence.
- **Consecutive Bit Patterns**—Defines the test patterns with repeating patterns.
- **Clock**—Generates a clock-like pattern.
- **All 1's**—Generates an all-ones test pattern that usually feeds into a coder or scrambler.
- **All 0's**—Generates an all-zeros test pattern that usually feeds into a coder or scrambler.
- **Encoder and Scrambler**—JNEye supports the following encoders and scramblers: **8B/10B**, **64B/66B**, **64B/67B**, and **128B/130B**.

- **Custom**—Click the open-file dialog button to select a custom test pattern file.

Figure 2-7: Custom Test Pattern File Browser Button



The custom pattern files are in the following formats:

- **Hexadecimal**—Hexadecimal strings start with **0x**. For example, a PRBS-7 test pattern can be specified by 0x8cd501fbe7ae1ba62b05e3b64a4272d0. The custom file name must have a **.hex** extension.
- **Binary**—Binary strings have a format such as "001000111…". Blank characters and new lines/returns are allowed in the input binary string file. The custom file name must have a **.bin** extension.

Note: The custom test pattern has a maximum text length of 262,142 characters (about 1M bits with a hexadecimal text format or about 246K bits with a binary text format). Altera recommends that the test pattern string (hexadecimal or binary) is specified in a single row without spaces, especially for long custom test patterns. If a custom test pattern is input with multiple lines of text, the line returns or end-of-line control characters on each line of text are counted as an item or entry by the text parser.

Reference Clock

Specifies the reference clock that feeds into the transmitter. The supported clock frequencies are shown in MHz. By default, the reference is assumed to be ideal without any noise or jitter. You can configure and specify the reference clock characteristics by clicking **Reference Clock Option**.

The reference clock can be fed to a transmitter with or without enabling a phase-locked loop (PLL) module. When the transmitter PLL is disabled or not present, the reference clock noise and jitter directly affects the serial output signal.

With integer PLLs, JNEye supports an integer divider ratio between the data rate and the reference clock frequency. If the ratio is not an integer, the reference clock frequency is rounded to the closest integer-divided-ratio frequency. The actual reference clock frequency used in the simulation is displayed in the message box next to the pull-down menu. With fractional-N PLLs, fractional divider ratios are allowed.

In the simulation with specific transmitter devices, such as Arria 10 GX/SX/GT, Stratix V GT, Stratix V GX, and Arria V GZ devices, the supported data rate to reference clock divider ratios are limited. If a specific combination of data rate, PLL divider ratio, and reference clock frequency cannot be found, the reference clock used in the simulation can be further adjusted.

The reference clock frequencies listed are commonly used in most serial link protocols. If you cannot find the exact reference clock frequency from the list, you can add your reference clock frequency with the following procedure:

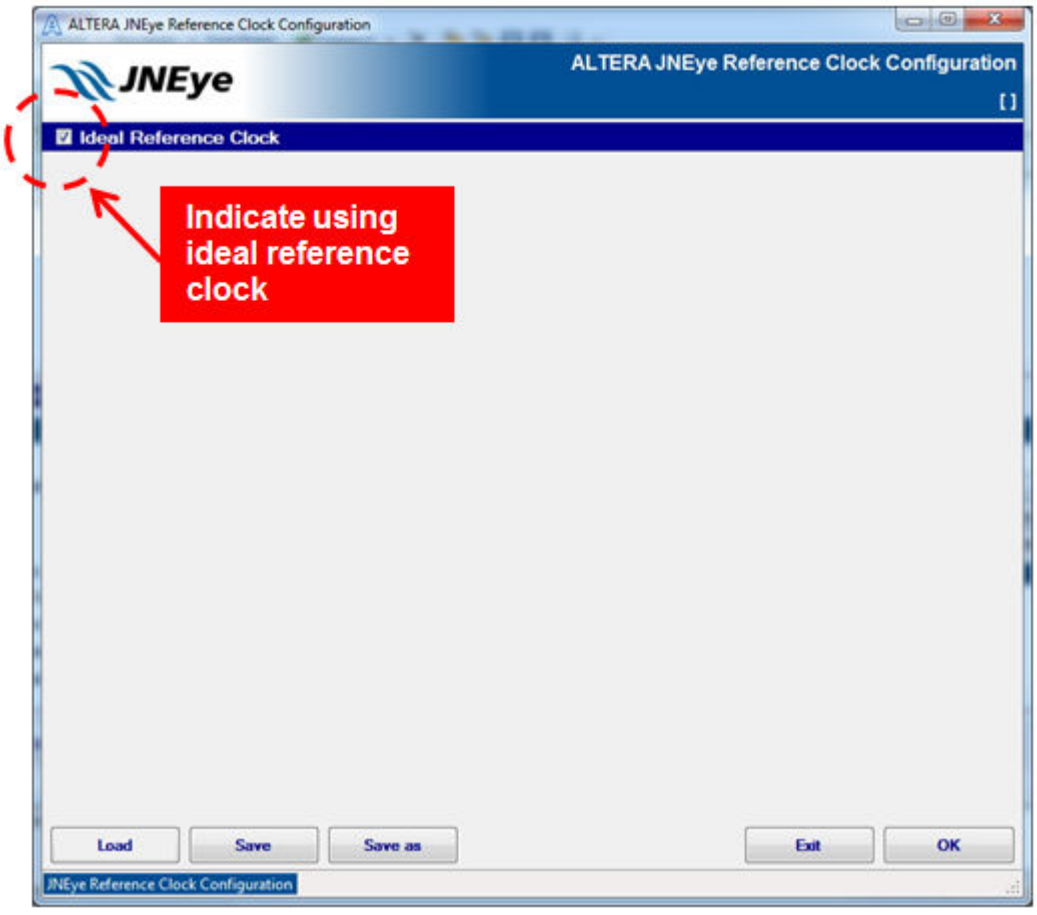
1. Close JNEye.
2. Navigate to the JNEye installation directory. Typically, JNEye is installed in **C:\altera\15.0\jneye**.
3. Under the **Database** folder, find **RefCLK_List.jnetxdata**.
4. Edit the file by adding your desired reference clock frequencies.
5. Save the change and exit the editor.
6. Restart JNEye.

Reference Clock Option

The reference clock option user interface allows you to configure the characteristics of the reference clock used in the simulation. The reference clock can be specified with the following methods:

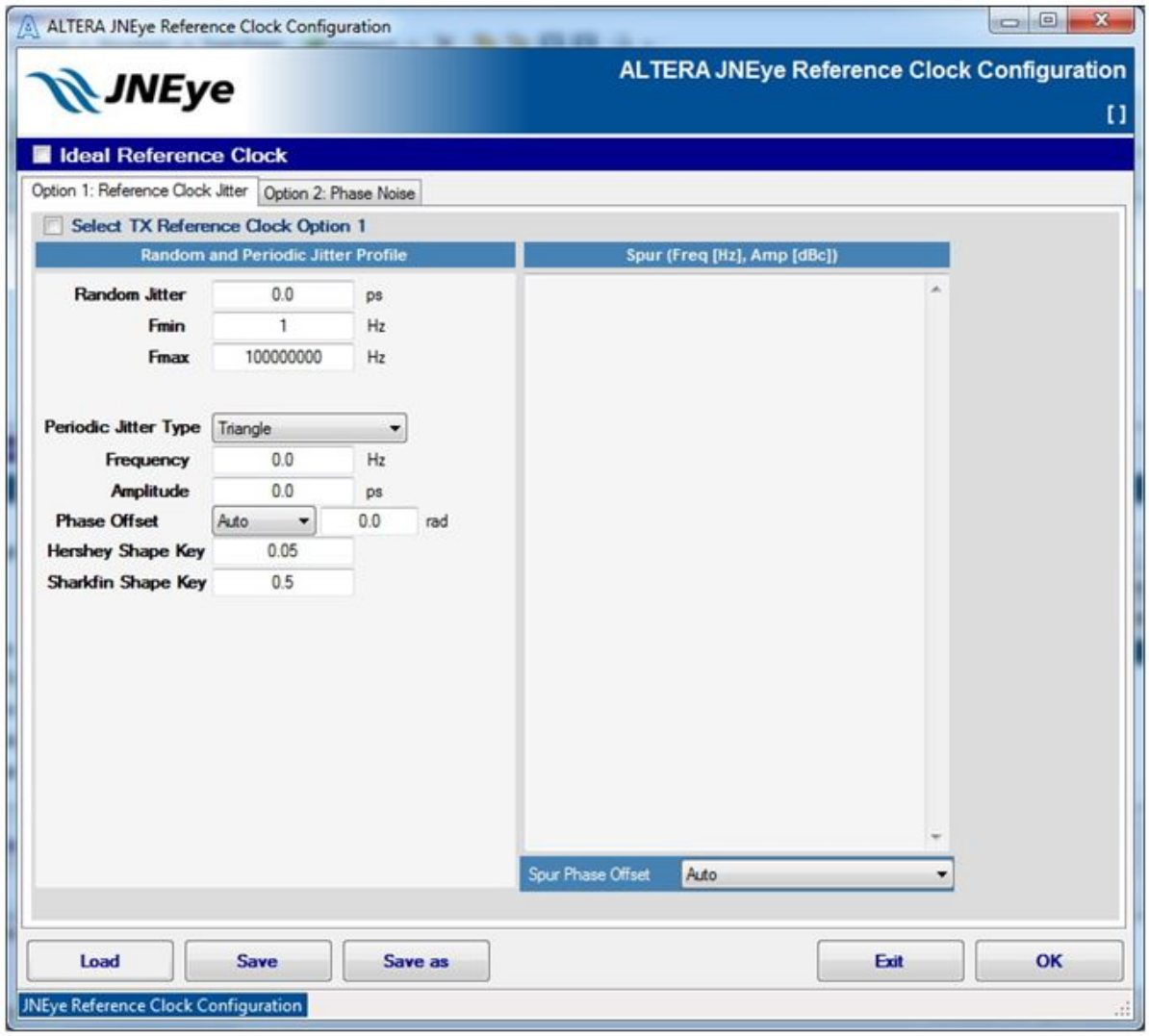
- **Ideal Reference Clock**—With this setting, the reference clock is ideal without any noise or jitter.

Figure 2-8: Ideal Reference Clock Setting



- **Option 1: Reference Clock Jitter**

Figure 2-9: Reference Clock Option 1: Reference Clock Jitter



Option 1 configures the reference clock with the following options:

- **Random Jitter**— Specify the frequency range (in ps).

  Note: Altera recommends that the maximum frequency range (f_{MAX}) of the phase noise be set to the reference clock frequency. If the f_{MAX} is less than the reference clock frequency, JNEye uses linear extrapolation to calculate the phase noise at f_{MAX}, which can lead to inaccurate results.
- **Periodic Jitter Type**—Specify the shape profile, frequency (in Hz), and amplitude (in ps). The shape profile can be:
  - Triangle
  - Hershey with programmable Hershey shape parameter
  - Sharkfin with programmable Sharkfin shape parameter
  - Sinusoidal
- **Spurs**—Specify clock spectrum spurs with individual frequency (in Hz) and amplitude (in dBc). For example, if the reference clock has three spurs: –110 dBc at 100 KHz, –90 dBc at 1 MHz, and –80 dBc at 10 MHz, you can input the following text into the Spurs text box:

```
100e3 -110
1e6 -90
10e6 -80
```

- **Spur Phase Offset**

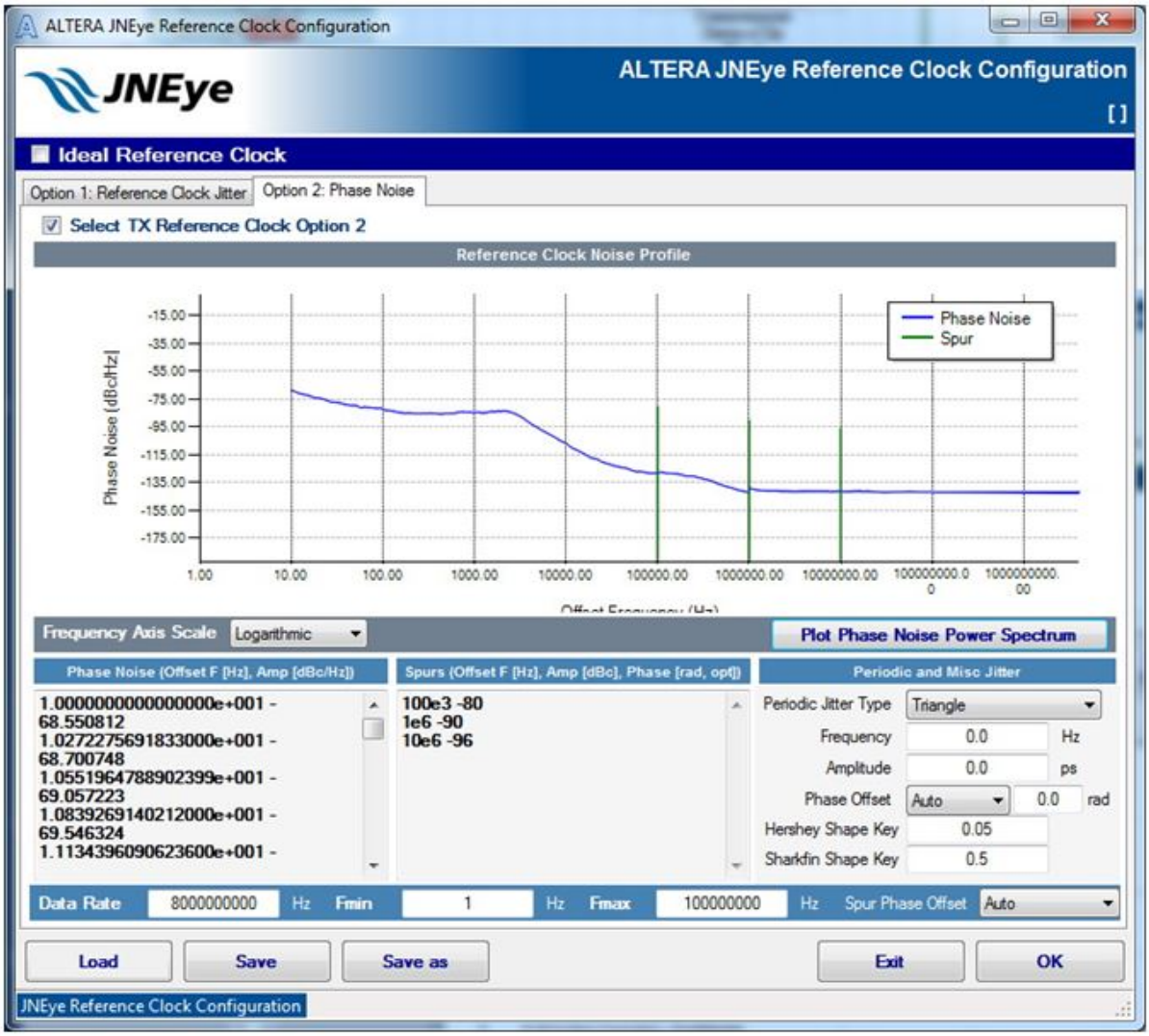
  Use the Spur Phase Offset pull-down menu to configure the initial phase of spur noises. The options are:

  - **Auto**—JNEye automatically selects the default initial spur noise phase. The default initial spur phase is 0 rad.
  - **Random**—JNEye randomly sets the initial spur noise phases.
  - **Zero**—JNEye sets the initial spur noise phase to 0 rad.
  - **Specified**—You can manually specify the initial spur phase individually by adding the phase value after the amplitude value. The following example shows the initial spur noise phases are 1.0, 2.0, and 3.0 rad.

```
100e3 -110 1.0
1e6 -90 2.0
10e6 -80 3.0
```

- **Option 2: Phase Noise**

Figure 2-10: Reference Clock Option 2: Phase Noise



Option 2 configures the reference clock with the following options:

- **Phase Noise**—Specify reference clock jitter using a phase noise profile. Reference clock phase noise is specified with the noise power spectrum described with frequency and amplitude. The above figure demonstrates a phase noise profile with a measured reference clock phase noise data set.

  Note: Altera recommends that the maximum frequency range (f_{MAX}) of the phase noise be set to the reference clock frequency. If the f_{MAX} is less than the reference clock frequency, JNEye uses linear extrapolation to calculate the phase noise at f_{MAX}, which can lead to inaccurate results.
- **Spurs**—Specify clock spectrum spurs with individual frequency (in Hz) and amplitude (in dBc). For example, if the reference clock has three spurs: –80 dBc at 100 KHz, –90 dBc at 1 MHz, and –96 dBc at 10 MHz, you can input the following text into the text box:

```
100e3 -80
1e6 -90
10e6 -96
```

- **Spur Phase Offset**—Same as in **Option 1 Reference Clock Jitter**.
- **Periodic Jitter Type**—Same as in **Option 1 Reference Clock Jitter**.
- **Plot / Update Plot**—You can plot the input phase noise and spurs in the plotting area and confirm the reference clock characteristics.

Link Optimization Method

JNEye can find optimal transmitter and receiver equalization settings with a user-specified link configuration.

Note: The TX/RX joint link optimization function is specific to JNEye and may not be supported by the transmitter and receiver devices.

Table 2-4: Link Operation Modes Supported by JNEye

Transmitter Mode	Receiver Mode	Notes
Manual	Manual	Both TX and RX equalizations are manually set.
Auto / Auto with Manual Starting Point	Manual	JNEye finds optimal TX equalization setting. RX EQ setting is manually set.
Manual	Auto	TX EQ is manually set. JNEye finds optimal RX EQ setting.
Auto / Auto with Manual Starting Point	Auto	JNEye finds both TX and RX EQ settings.

JNEye has four link optimization methods for finding the optimal link setting, such as a transmitter pre-emphasis and receiver CTLE and DFE with a given link configuration.

- **FIR => CTLE => DFE**— (default) Optimizes the link performance by finding the optimal transmitter setting, receiver equalization setting, or both. This method prioritizes the transmitter equalization, such as pre-emphasis, de-emphasis, or FIR-based, over receiver equalization schemes. However, the optimization algorithm is also capable of detecting and utilizing optimal receiver equalization. In practice, this usually implies that most of the "heavy-lifting" in channel compensation is performed by the transmitter equalization.
- **FIR => CTLE & DFE**—Extends the **FIR => CTLE =>DFE** method by enabling RX DFE (Decision Feedback Equalizer) when RX optimization is performed. This method exploits DFE capabilities by possibly reducing the channel compensation from CTLE (depending on the channel characteristics).
- **CTLE => FIR => DFE**—Prioritizes the receiver's CTLE capability over the transmitter's equalization. Most of the channel compensation is performed by the receiver's CTLE while the TX equalization provides additional compensation if needed. RX DFE is adapted in the final stage. This method is supported in non-IBIS-AMI devices. For Altera transmitters, you can manually set initial TX FIR configurations so the link optimizations can yield better solutions more quickly when the initial conditions are proper.
- **CTLE => FIR & DFE**—Extends the **CTLE => FIR => DFE** method by joint-optimizing TX pre-emphasis/FIR and RX DFE. This method allows co-optimization between the TX FIR and RX DFE. For Altera transmitters, you can manually set the initial TX FIR configurations so the link optimizations can yield better solutions more quickly when the initial conditions are proper.

Use the following guidelines for choosing the best link optimization method:

- **FIR => CTLE => DFE** is a good choice for most applications or channels for time efficient link optimizations. It is the default link optimization method in JNEye.
- For heavy insertion loss channels such as when insertion loss > 25 dB at Nyquist frequency, **FIR => CTLE => DFE** provides good coverage.
- For strong impedance discontinuities, **CTLE => FIR => DFE** methods provide better performance in general.
- For large crosstalk noises, choose **FIR => CTLE & DFE** for high loss channels or **CTLE => FIR & DFE** for moderate loss applications.

Notes:

- JNEye supports link optimization for selected IBIS-AMI models for the link optimization modes and the methods shown above. Refer to the IBIS-AMI model support sections for details.
- For a transmitter equalization sweep simulation, JNEye provides batch simulation capability using the **JNEye Batch Simulation Controller** tool. Refer to the *JNEye Batch Simulation Controller* section for details.

FOM of Link Optimization

Use this menu to select the figure of merit (FOM) for optimizing the serial link. There are three options: **Area**, **Width**, and **Height**. The signal conditioning mechanisms, which include transmitter pre-emphasis, de-emphasis, and receiver equalizers, use these selections to optimize the waveform so that it has the best eye diagram opening in terms of area, width, or height.

Compliance Mask

JNEye plots link compliance eye diagram masks after the simulations are completed. Use a compliance mask to examine whether the waveform or eye diagram meets the receiver's requirements at certain conditions (such as BER target). PCI-Express 8GT receiver eye masks are provided.

Note: Device intrinsic jitter can be included in the link simulation by using the Characterization Data Access function in JNEye. When both transmitter and receiver jitter are extracted from the Characterization Data Access and included in the simulation, the simulation results at the end of

the link represent the link margin at the specified bit error rate (BER) target. Link margin simulation using transmitter and receiver jitter provides better accuracy than the conventional eye mask method.

Eye Diagram Mask Designer

JNEye supports custom eye diagram mask definition. When the **Eye Diagram Mask Designer** option is selected, the custom eye diagram mask configuration window opens. You can then specify the dimension of the eye diagram mask. The custom eye diagram mask is used in the simulation. Two eye diagram mask types are supported:

Figure 2-11: Hexagon-Shaped Eye Diagram Mask Editor

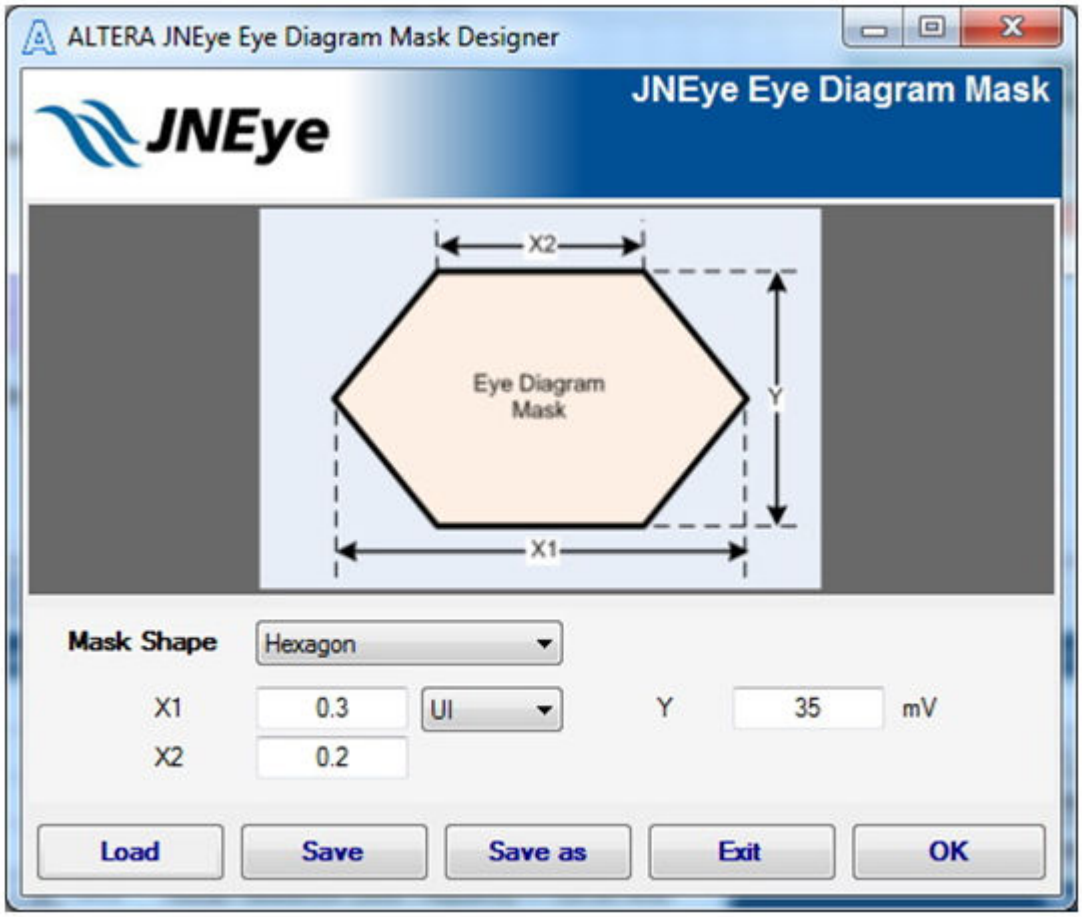
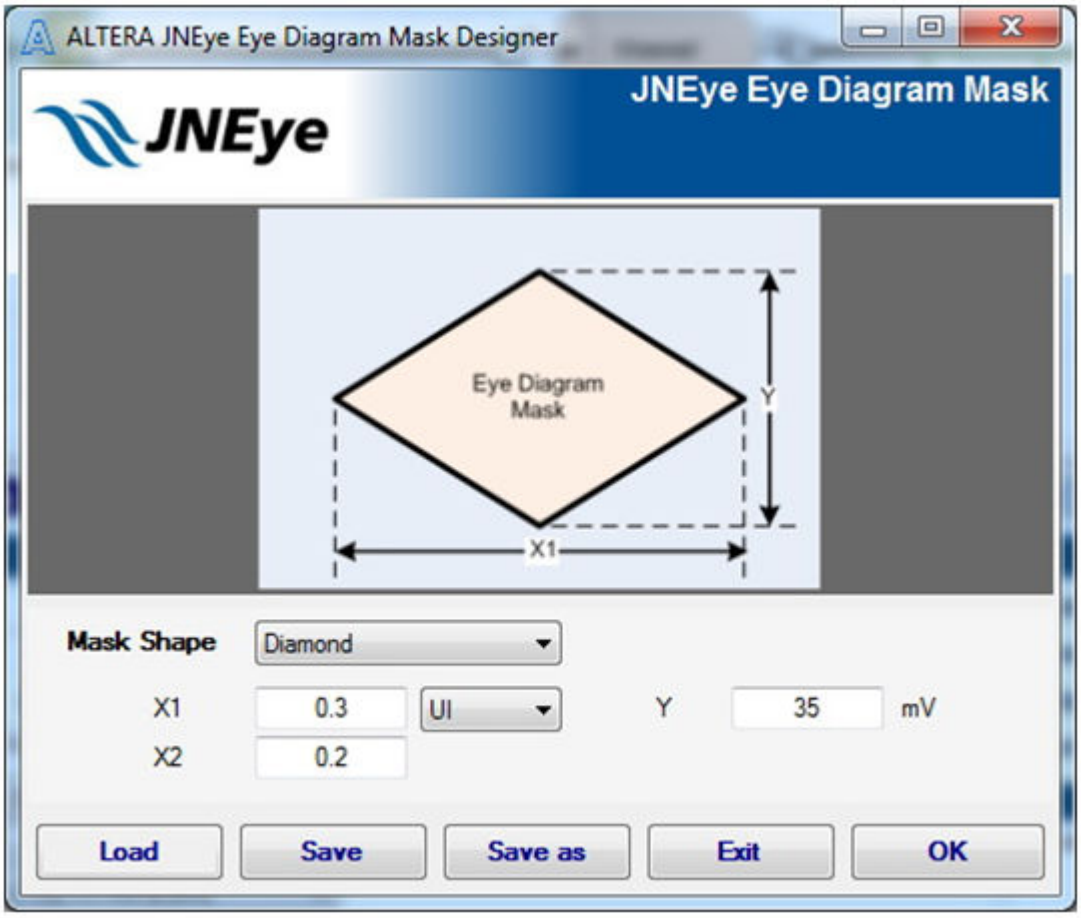


Figure 2-12: Diamond-Shaped Eye Diagram Mask Editor



A custom eye diagram mask can be saved and loaded for future use.

Project Name

A user-defined name for the current task/project. Currently, the session name is the saved user configuration file name when the simulation configuration is saved.

Notes:

- The simulation results are automatically written to a directory with the same project name.
- The location of the output directory can be configured as a) the same location as the project configuration file (.jne/.jneschm) (this is the default), or b) a location you specify in the System Options. Refer to the System Options section for details.

Simulation Mode

JNEye provides three simulation modes (statistical, full waveform, and hybrid) to meet your simulation and link analysis preferences and needs. Hybrid mode is the default.

Table 2-5: Simulation Modes

PDF = Probability Density Function

	Statistical Mode	Full Waveform Mode	Hybrid Mode (Default)
Simulation Method	Statistical Method	Time-domain Method	Time-domain and Statistical Methods
Jitter Injection and Simulation	Statistical Domain (PDF- based)	Time Domain	Mixed Domain (Time Domain and PDF-based)
Noise Injection and Simulation	Statistical Domain (PDF- based)	Time Domain	Mixed Domain (Time Domain and PDF-based)
Simulation Speed (to meet your specified BER target)	Fast	Slow	Optimal
Accuracy	Lower	Best	Optimal
Recommended Simulation Length	N/A (You do not need to specify simulation length in statistical mode.)	>500,000 bits	~60,000 bits

Further information and comparisons among the three simulation modes can be found in the following papers:

1. *Comparison of Two Statistical Methods for High-Speed Serial Link Simulation* by M. Shimanouchi, M. Li, and H. Wu. DesignCon, 2013, Santa Clara, CA.
2. *Advancements in High-Speed Link Modeling and Simulation* by M. Li, M. Shimanouchi, and H. Wu. IEEE Custom Integrated Circuits Conference, 2013.
3. *High-Speed Link Simulation Strategy for Meeting Ultra Long Data Pattern under Low BER Requirements* by H. Wu, M. Shimanouchi, and M. Li, DesignCon, 2014, Santa Clara, CA.

Output Options

- **Data Viewer**—When simulation is complete, a new JNEye Data Viewer opens and the results are shown. The simulation results can be loaded and viewed at a later time with JNEye Data Viewer.
- **Data Viewer with Image Output**—When simulation is complete, all the simulation results are also saved as image files that can be used in documentation. JNEye supports three image output options: PNG, JPEG, and GIF. The saved images are located in the same directory as the simulation results for each project.

Test Point Options

JNEye provides the following default test point options:

- **Data Latch Only**—(default option) Simulation results at the data latch will be saved and displayed. Data latch can be at DFE output, CTLE output, or input stage of receiver depending on the link or device configuration. Custom test points will be neglected and the simulation results at test points will not be shown.
- **TX/Channel/CTLE-/DFE-Latch**—JNEye automatically sets up to four test points for the link:
  - **Transmitter output**—If a transmitter package model is present (for example, the package model is embedded, as in Altera devices and PCI-Express 8GT) or external (for example, using the "Custom" package option), the output appears after the package model. If no package model is present, the output appears at the transmitter output.
  - **Channel output**—The second test point is at the end of channels.
  - **CTLE output**—If you enable the receiver CTLE, the third test point is at the output of the CTLE.
  - **DFE output**—The fourth test point is at the output of the receiver DFE.

  Note: Custom test points are neglected with this test point option.
- **Custom Test Point and Data Latch**—JNEye plots the output at custom test points and the final data latch point.

Probe Type

JNEye provides two type of probes:

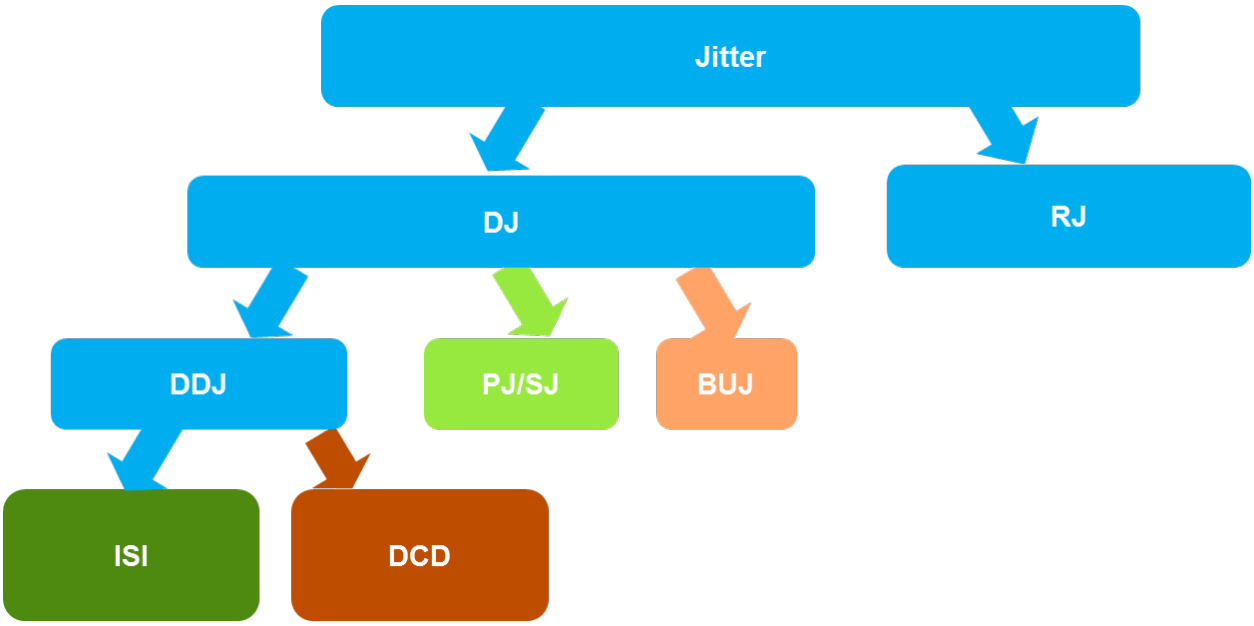
- **Ideal**—With an ideal probe, the waveform, signal, or eye diagram is plotted by assuming that the link is terminated with an ideal 50 ohms termination at the probe location.
- **High-Impedance**—With a high-impedance probe, the waveform, signal, or eye diagram is plotted by emulating a high-impedance probe sensing the probe location.

Jitter Analysis Options

JNEye can perform jitter decomposition and analysis on a waveform at specified test points. The jitter analysis feature is in the beta testing stage in the JNEye 15.0 release.

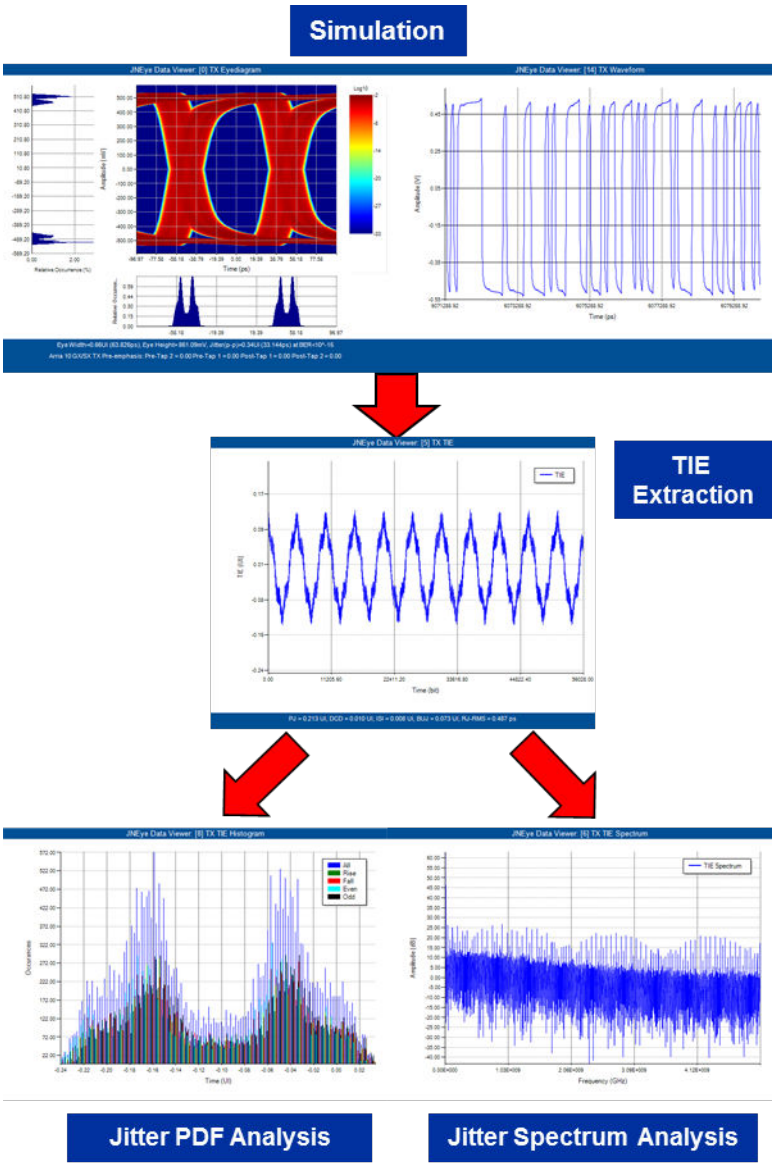
- **Disable**—Jitter analysis is disabled.
- **Jitter Component**—Using proprietary algorithms, JNEye performs a series of spectrum and probability density function (PDF) analyses on the time-interval-error (TIE) record of the simulated waveforms. The jitter decomposition algorithms extract various jitter components as shown in the following figure.

Figure 2-13: Jitter Component Supported in JNEye Jitter Analysis Feature



The jitter decomposition process (conceptual) is shown in the following figure.

Figure 2-14: Jitter Decomposition Process (Conceptual)



In JNEye 15,0, the following jitter components are extracted and reported:

- **PJ**—Periodic jitter (peak-peak)
- **DCD**—Duty cycle distortion (peak-peak)
- **ISI**—Inter-symbol interference (peak-peak)
- **BUJ**—Bounded uncorrelated jitter (peak-peak)
- **RJ-RMS**—Random jitter (RMS)

Note: In JNEye 15.0, jitter analysis is available in Hybrid simulation mode only.

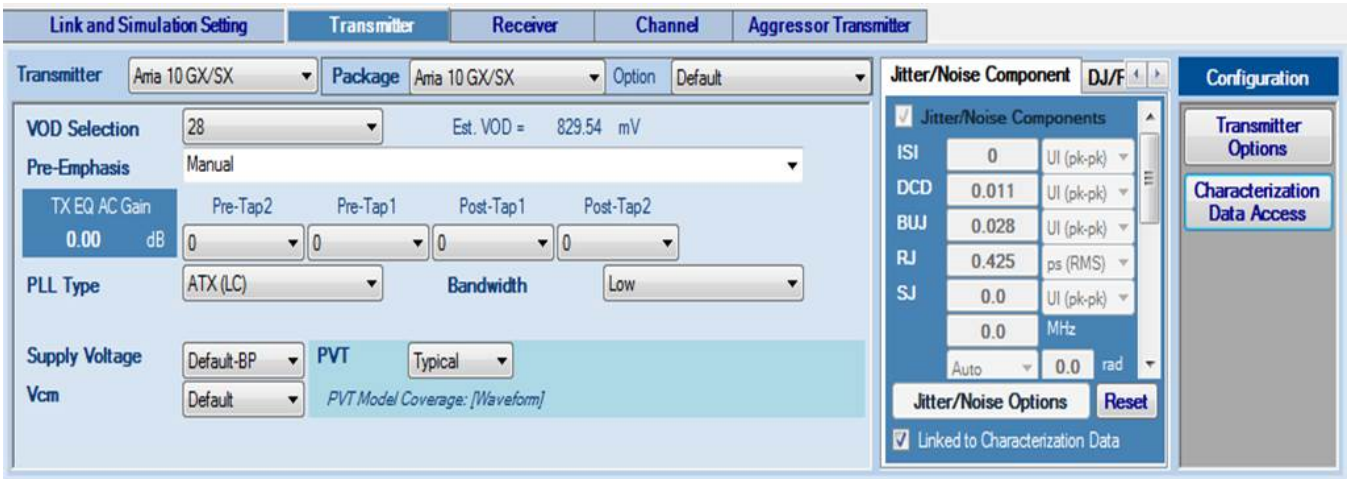
Related Information

- **JNEye Batch Simulation Controller** on page 2-129
- **HST Jitter and BER Estimator Tool User Guide for Stratix IV GT and GX Devices**

Transmitter Setting

The transmitter generates signals based on the transmitter clock and test pattern conditions.

Figure 2-15: JNEye Transmitter Settings



Transmitter

The following transmitter types are supported:

- Stratix V GX
- Arria V GZ
- Arria 10 GX/SX
- Arria 10 GT
- IBIS-AMI
- Custom
- PCI Express 8GT

The transmitter type determines what other transmitter settings you can select. When a transmitter is chosen, it is automatically inserted into the Link Designer, ready to connect to other link components.

Package

Select a package type for the transmitter device. For Altera products and IBIS-AMI models, the package models are included in the device models. For Custom devices, the package model is specified in the channel setting. When you select the Custom package type (for any transmitter devices), the embedded package model (if available) is disabled. You can then add a channel component (such as an S-parameter) with type Package in the Link Designer workspace. The Custom package model must be placed next to the transmitter module so it can be simulated and analyzed correctly. If you choose the Custom package type but do not add a channel component with Package type to the Link Designer workspace, the transmitter is simulated without any package model.

JNEye comes with the following transmitter package models:

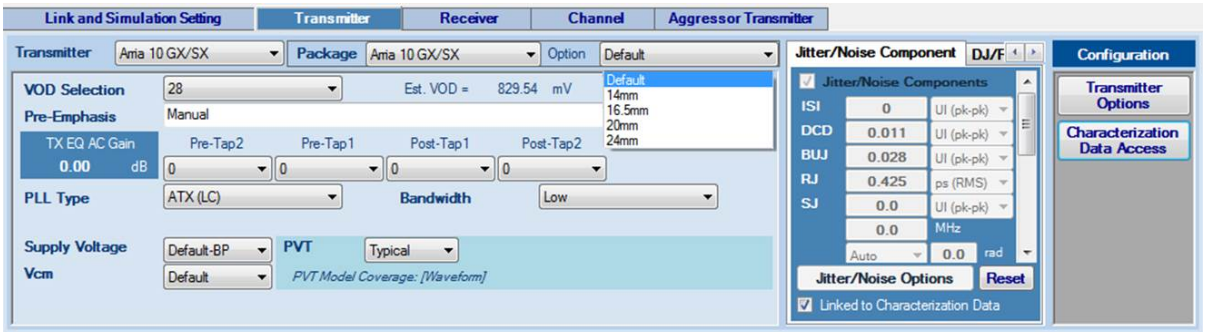
- Stratix V GX
- Arria V GZ
- Stratix V GT
- Arria 10 GX/SX

  Options: Additional package models (shown in the following figure) are available for Arria 10 devices. The package model is specified as its trace length inside the package. These models are chosen to cover the range of package trace lengths in Arria 10 transceiver transmitters.

  - **Default**—The default package model is same as the 14 mm option
  - **14mm**
  - **16.5mm**
  - **20mm**
  - **24mm**

  Contact your Altera's representative if you would like to know how to pair your design with the Arria 10 package model options.

Figure 2-16: Arria 10 Transmitter Package Options



- Arria 10 GT—Same options as Arria 10 GX/SX
- PCI-Express 8GT

VOD Selection

Select the VOD (differential output voltage) for the transmitter. VOD selections can be either by voltage level or by index, depending on the transmitter selected. For supported devices, the target VOD value is displayed in the Transmitter tab page. The VOD value depends on the device type, supply voltage, and PVT.

Pre-Emphasis

Select or specify the transmitter pre-emphasis, de-emphasis, or TX-FIR configuration in one of the following modes:

- **Auto**—JNEye uses its link optimization algorithm to find the optimal transmitter FIR settings.
- **Auto with Manual Starting Point**—Specify the initial TX pre-emphasis or FIR configuration. JNEye's link optimization engine uses the TX settings as initial conditions.
- **Manual**—For non-Altera devices, you can manually input the tap coefficients. For Altera devices, select individual FIR levels from the menus for each FIR tap. The FIR selection for Altera devices is VOD dependent. Therefore, changing the VOD or device type can reset the TX FIR menu contents. For a generic transmitter type, a set of typical FIR coefficients is included in the pull-down menu.
- **Off**

Estimated TX EQ AC Gain

Select pre-tap and post-tap values to estimate the AC gain in dB scale. The TX EQ AC gain is calculated as the gain between the DC (0 Hz) and the Nyquist frequency of the link, assuming a FIR type of transmitter pre-emphasis scheme.

Note: This is a rough analytical estimate of TX EQ AC gain that may differ from the actual AC gain generated by the transmitter.

PLL Type and Bandwidth

Select the type and bandwidth of the PLL used in the transmitter to generate the transmitter clock.

- **Ideal Clock**—The default PLL setting. The PLL is disabled and the clock is passed from the external reference clock.
- For **Altera transmitters**, PLL models and configurations are automatically set based on the following settings:
  - Data rate
  - Reference clock frequency
  - Oscillator type:
    - Stratix V GX and Arria V GZ—ATX (LC) or CMU
    - Stratix V GT—ATX (LC)
    - Arria 10 GX/SX/GT—ATX (LC), Fractional PLL, or CMU
  - PLL bandwidth
  - Altera transmitter PLL configurations such as internal divider ratios

  Altera recommends that you follow Altera's reference clock selection and PLL configurations recommendations when setting up the transmitter PLL. Without following the reference clock and PLL guidelines, you might operate and simulate an unstable PLL and see unexpected results.
- For **Custom transmitters**, PLL models and configuration are set automatically based on settings similar to that of Altera PLLs while more comprehensive PLL configuration capabilities are under development. With custom transmitters, the VCO can be either LC type or ring oscillator (Ring) type. More PLL to reference clock divider ratios are supported in the custom PLL type. Follow Altera's PLL and reference clock guidelines when setting up transmitter PLLs to avoid unexpected results.
- PLL is currently not supported for IBIS-AMI transmitters.

Supply Voltage

For supported devices, you can choose the supply voltage. In JNEye 15.0, the Arria 10 GX/SX/GT transmitter model provides the following supply voltages:

- **Default-BP**—Supply voltage for backplane applications that have a dependency on the data rate setting
- **Default-C2C**—Supply voltage for chip-to-chip applications that have a dependency on the data rate setting
- **0.9 V** (Arria 10 GX/SX/GT)
- **1.0 V** (Arria 10 GX/SX/GT)
- **1.1 V** (Arria 10 GT)

V_{cm}

V_{cm} is the common voltage of the transmitted signal.

PVT

Select the process, voltage, and temperature (PVT) models for the selected transmitter device. PVT model support varies depending on device type, device data availability, and model coverage. A message is shown on the Transmitter tab page to indicate the PVT model coverage. Transmitter PVT model coverage and conditions are shown in the following table.

Table 2-6: Transmitter PVT Model Coverage

Transmitter Type	Waveform PVT Model	Jitter/Noise PVT Model
Stratix V GX	Typical	Process: Typical/Fast/Slow Voltage: Typical/High/Low Temperature: –40°C to 100°C
Arria V GZ	Typical	Process: Typical/Fast/Slow Voltage: Typical/High/Low Temperature: –40°C to 100°C
Stratix V GT	Typical	Process: Typical/Fast/Slow Voltage: Typical/High/Low Temperature: 0°C to 100°C
Arria 10 GX/SX	Typical/Fast/Slow	Typical
Arria 10 GT	Typical/Fast/Slow	Typical
IBIS-AMI	Provide by IBIS-AMI model	Provide by IBIS-AMI model
Custom	None	None
PCI-Express 8GT	None	None

JNEye to Quartus II Parameter Translation for Arria 10 GX/SX/GT Transmitters

The following table provides a translation from JNEye Arria 10 GX/SX/GT transmitter parameter names to the equivalent Quartus II parameter names. Use the Quartus II software to transfer optimum device settings from a JNEye simulation to an actual device configuration.

Table 2-7: JNEye to Quartus II Parameter Translation for Arria 10 GX/SX/GT Transmitters

JNEye Name	Quartus II Name
Vod Selection	Transmitter Output Swing Level
Post-Tap 1 (1)	Transmitter Pre-Emphasis First Post-Tap Magnitude
Post-Tap 2 (1)	Transmitter Pre-Emphasis Second Post-Tap Magnitude
Pre-Tap 1 (1)	Transmitter Pre-Emphasis First Pre-Tap Magnitude
Pre-Tap 2 (1)	Transmitter Pre-Emphasis Second Pre-Tap Magnitude
Sign of Post-Tap 1 (1)	Transmitter Pre-Emphasis First Post-Tap Polarity (2)
Sign of Post-Tap 2 (1)	Transmitter Pre-Emphasis Second Post-Tap Polarity (2)
Sign of Pre-Tap 1 (1)	Transmitter Pre-Emphasis First Pre-Tap Polarity (2)
Sign of Pre-Tap 2 (1)	Transmitter Pre-Emphasis Second Pre-Tap Polarity (2)
PLL Type • ATX(LC) • Fractional PLL • CMU	Quartus II PLL Type • Arria 10 Transceiver ATX PLL • Arria 10 fPLL • Arria 10 Transceiver CMU PLL
PLL Bandwidth	Bandwidth in PLL Configuration Options in selected PLL type

Jitter/Noise Component

The Jitter/Noise panel allows you to input or import jitter and noise parameters. JNEye provides extensive transmitter jitter and noise modeling and configuration capabilities.

The following figure shows the jitter decomposition diagram and the breakdown of jitter components.

(1) In JNEye when Pre-emphasis is selected as **Manual** or **Auto with Manual Starting Point**
(2) "0" = non-inverted which is positive tap selections in JNEye; "1" = inverted which is negative tap selections in JNEye.

Figure 2-17: Transmitter Jitter Decomposition

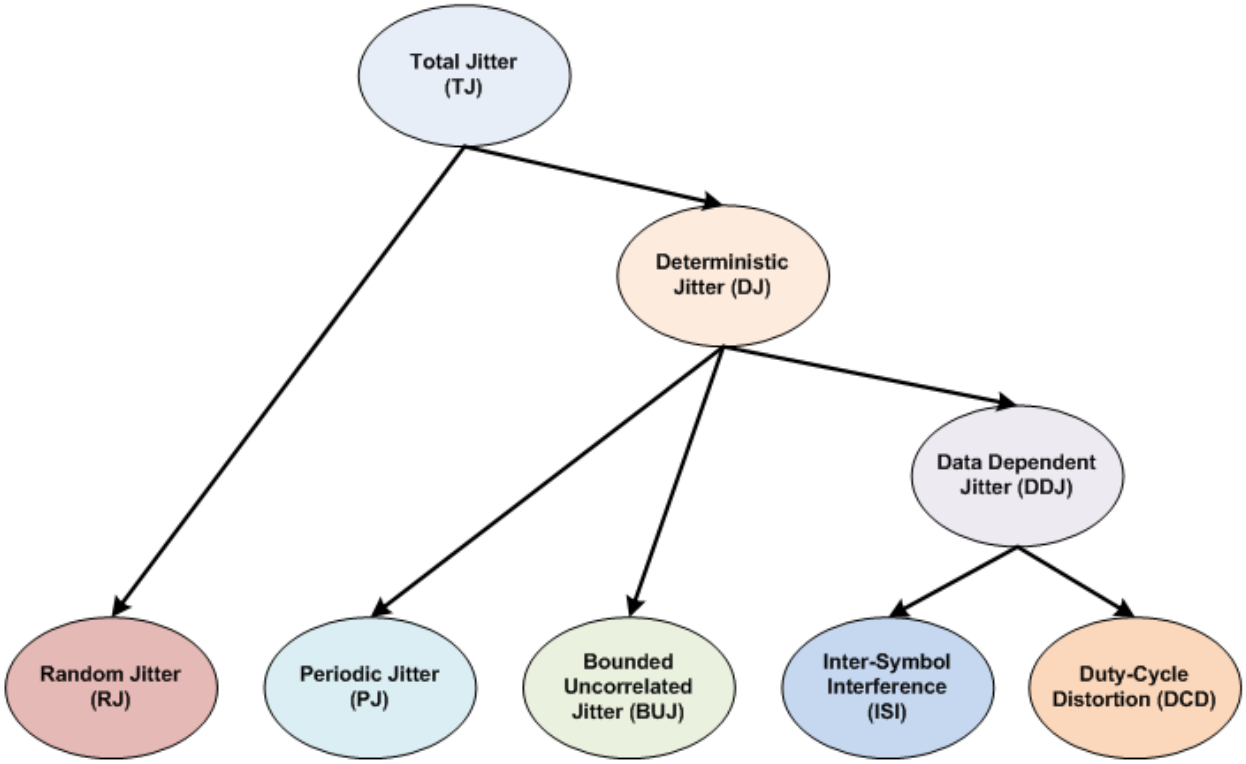


Table 2-8: Transmitter Intrinsic Jitter and Noise Types

Name	Description	Unit	Support in JNEye	Comments
DJ	Deterministic Jitter	Unit Interval (UI)	Yes	DJ can be generated using a uniform distribution, dual-Dirac, or truncated Gaussian method. Select the DJ generation method in the **Transmitter Jitter/Noise Options Window**. The default DJ method is dual-Dirac. DJ consists of periodic jitter, bounded uncorrelated jitter, inter-symbol interference, and duty-cycle distortion. The DJ value is used in the simulation when the DJ/RJ-DN/RN method is selected.
ISI	Inter-Symbol Interference	UI	Yes	ISI can be generated using a uniform distribution, dual-Dirac, or truncated Gaussian method. Select the ISI generation method in the **Transmitter Jitter/Noise Options Window**. The default ISI method is dual-Dirac.

Name	Description	Unit	Support in JNEye	Comments
DCD	Duty Cycle Distortion	UI	Yes	The DCD parameter models two types of jitter: Positive pulse width jitter (PPWJ) and Clock DCD. The PPWJ shortens or lengthens the logic 1 waveform. The Clock DCD emulates distorted clock waveform effects on the transmitter output waveform. You can select the DCD generation method in the **Transmitter Jitter/Noise Options Window**. The default DCD method is PPWJ – (shortened positive waveform).
BUJ	Bounded Uncorrelated Jitter	UI	Yes	Same as Deterministic Jitter. The default BUJ method is Uniform distribution.
RJ	Random Jitter	UI-RMS or ps-RMS	Yes	RJ is assumed to be Gaussian. RJ can be specified in either pico-second (ps-RMS) or UI-RMS.
SJ	Sinusoidal Jitter	Amplitude: UI Frequency: MHz	Yes	Sinusoidal jitter can be specified with amplitude and frequency.
DN	Deterministic Noise	mV	Yes	DN can be generated using a uniform distribution, dual-Dirac, or truncated Gaussian method. You can select the DN generation method in the **Transmitter Jitter/Noise Options Window**. The default DN method is uniform.
BUN	Bound Uncorrelated Noise	mV	Yes	Same as DN. The default method is Truncated Gaussian method with a Peak-to-RMS ratio of 14. You can select the BUN generation method and parameters in the **Transmitter Jitter/Noise Options Window**.
RN	Random Noise	mV-RMS	Yes	RN is assumed to be Gaussian.

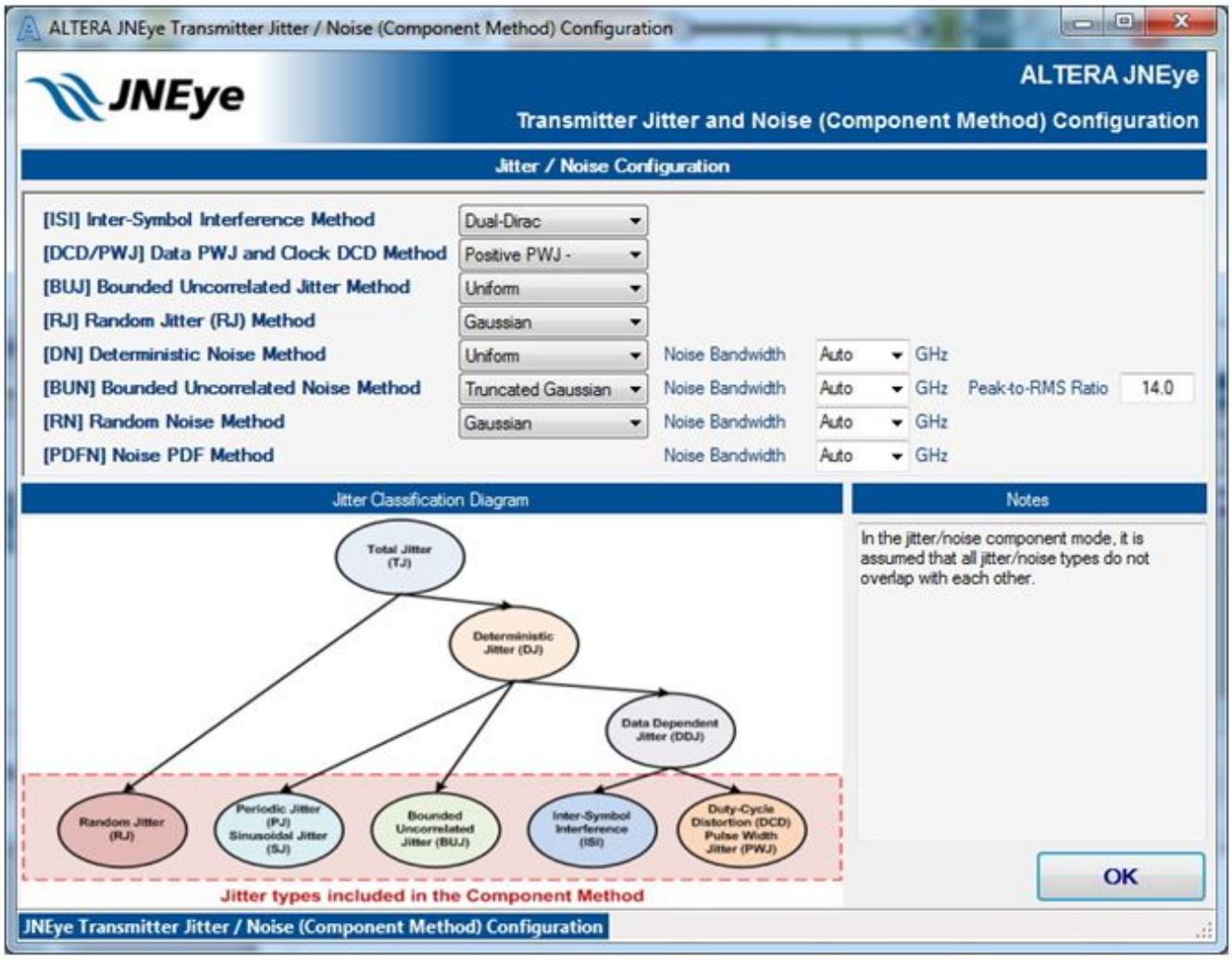
Name	Description	Unit	Support in JNEye	Comments
Jitter PDF	Jitter Probability Density Function (PDF)	Jitter amplitude, Probability (Jitter amplitude can be in absolute time or UI (unit interval) unit)	Yes	Jitter PDF defines the jitter probability density function. The input format is jitter amplitude in second and probability. The following is a jitter PDF example: -5e-12 1e-10 -4e-12 3e-7 -3e-12 1e-4 -2e-12 1e-2 -1e-12 0.29 0 0.4 1e-12 0.29 2e-12 1e-2 3e-12 1e-4 4e-12 3e-7 5e-12 1e-10
Noise PDF	Noise Probability Density Function	Noise amplitude, Probability	Yes	Noise PDF defines the noise probability density function. The input format is Noise amplitude in volt and probability. The following is a noise PDF example: -50e-3 1e-10 -40e-3 3e-7 -30e-3 1e-4 -20e-3 1e-2 -10e-3 0.29 0 0.4 10e-3 0.29 20e-3 1e-2 30e-3 1e-4 40e-3 3e-7 50e-3 1e-10

Click **Jitter/Noise Options** to further configure each jitter and noise type. There are two jitter/noise modes for JNEye's transmitters: **Jitter/Noise Component mode** and **DJ/RJ-DN/RJ mode**. Only one jitter/noise mode is active at a time and you must determine which mode to use in your simulations.

- **Jitter/Noise Component mode**—JNEye uses a flat jitter/noise structure that assumes no overlapping among all the jitter and noise components. Avoid double counting when inputting or importing jitter/noise figures. In the following figure, there are six specific jitter components: DCD, ISI, SJ, BUJ, RJ, and jitter PDF. The noise components DN, BUN, RN, and noise PDF must also be specified separately.

Figure 2-18: Specifying Transmitter Jitter and Noise in Jitter/Noise Mode

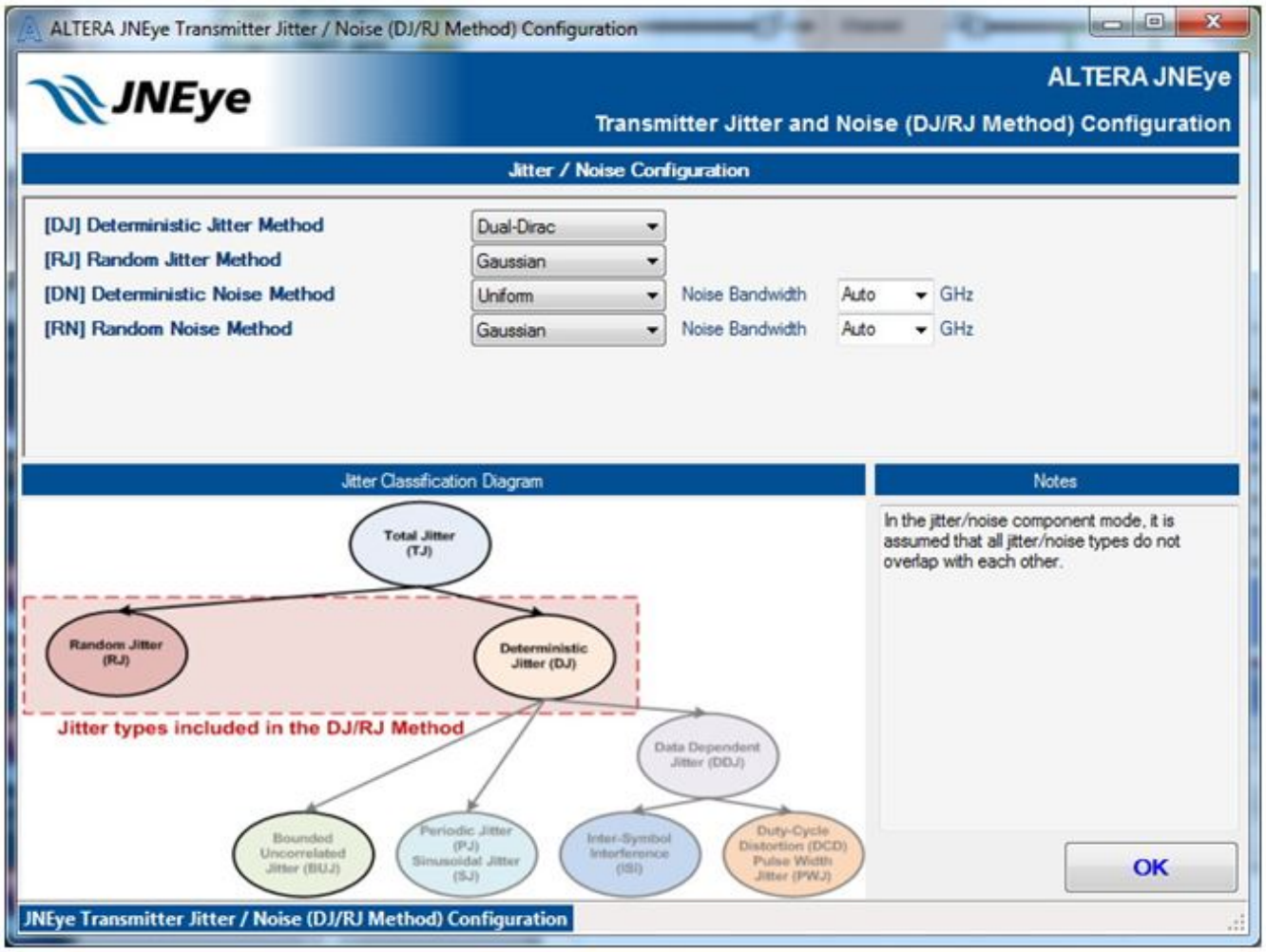
Figure 2-19: Transmitter Jitter/Noise Configuration in Jitter/Noise Component Mode



- **DJ/RJ-DN/RJ mode**—All deterministic jitter/noise components are included in DJ and DN.

Figure 2-20: Specifying Transmitter Jitter and Noise in DJ/RJ-DN/RJ Mode

Figure 2-21: Transmitter Jitter/Noise Configuration in DJ/RJ-DN/RJ Method



Note: Jitter specified in the Transmitter Noise/Jitter panel is the transmitter's *intrinsic jitter and noise*. Jitter specified in the Reference Clock configuration window is external reference clock jitter. You must distinguish between these two parts and avoid double-counting jitter from the same source.

Transmitter Options

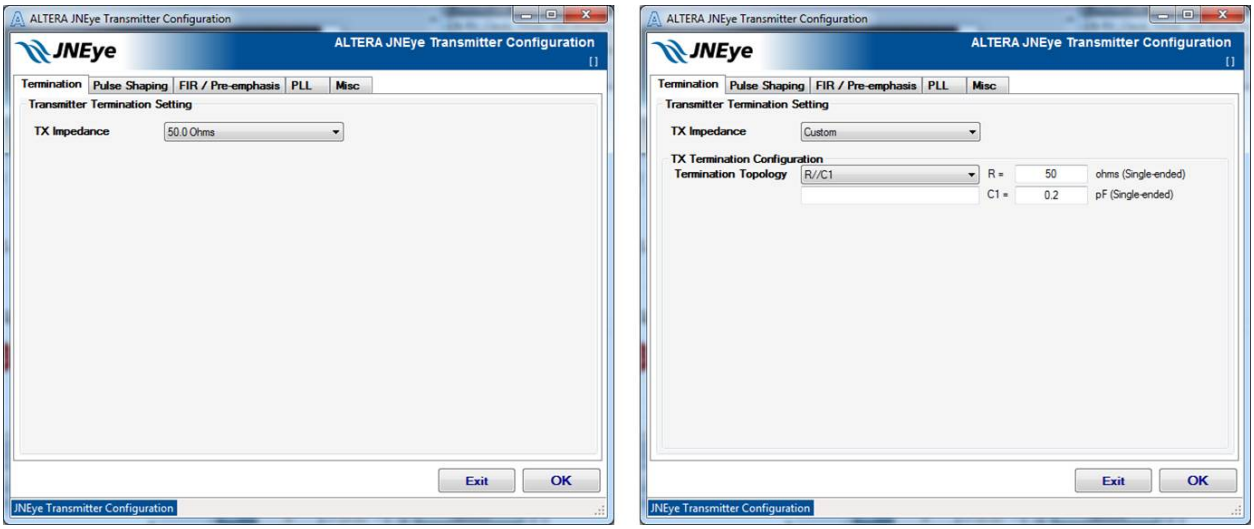
Transmitter options provide further configuration and setting options for transmitters. The additional options are only displayed or valid for transmitter devices that allow custom configurations.

Note: Not all Transmitter Options are available for all transmitter devices.

Termination tab

This section specifies the transmitter impedance.

Figure 2-22: Transmitter Advanced Options Window: Transmitter Termination



For selected Altera devices, use the **TX Impedance** pull-down menu to select a termination configuration. You can also customize the termination configuration by selecting the **Custom** option. When the **Custom** TX Impedance method is chosen, the termination can be configured as follows:

- **Ideal** TX termination—The transmitter is ideal with a 50 ohms (single-ended) termination.
- **Non-ideal** TX termination—Select one of the following options:
  - **R**—Transmitter impedance is modeled as a resistance R ohms (single-ended).
  - **R//C1**—Transmitter impedance is modeled as an RC network with a parallel resistor (in ohms) and a capacitance (in pF).
  - **File Input** (Frequency Real Imaginary)—Transmitter impedance is modeled by a frequency-dependent complex impedance table described in the input file.

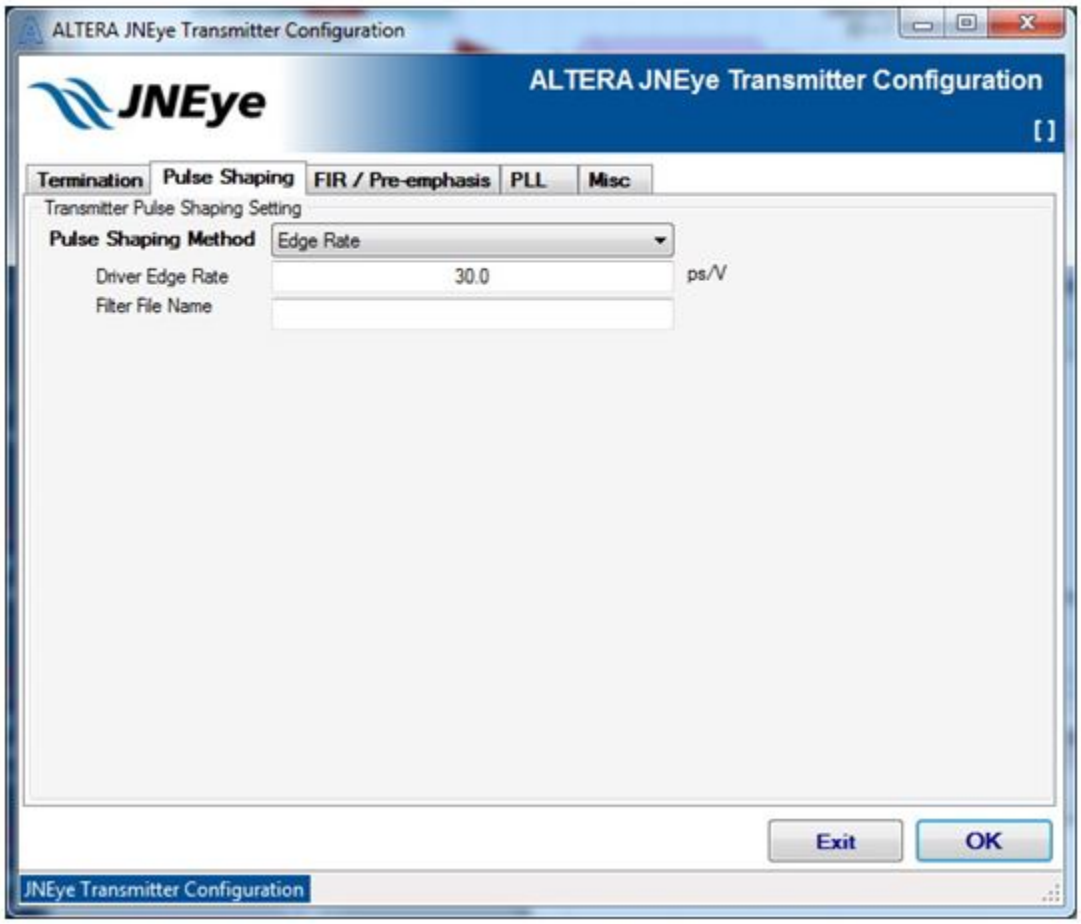
For an Altera transmitter, the default termination configurations are automatically selected and specified.

Pulse Shaping tab

JNEye supports two pulse shaping methods for Custom transmitters:

- **Edge Rate**—A pulse-shaping filter is generated by using a Gaussian low-pass filter that matches the specified edge rate.
- **S-parameter**—A pulse-shaping filter is specified by your S-parameter file. Only the differential insertion loss (for example, S_{dd21}), is applied in the pulse shaping.

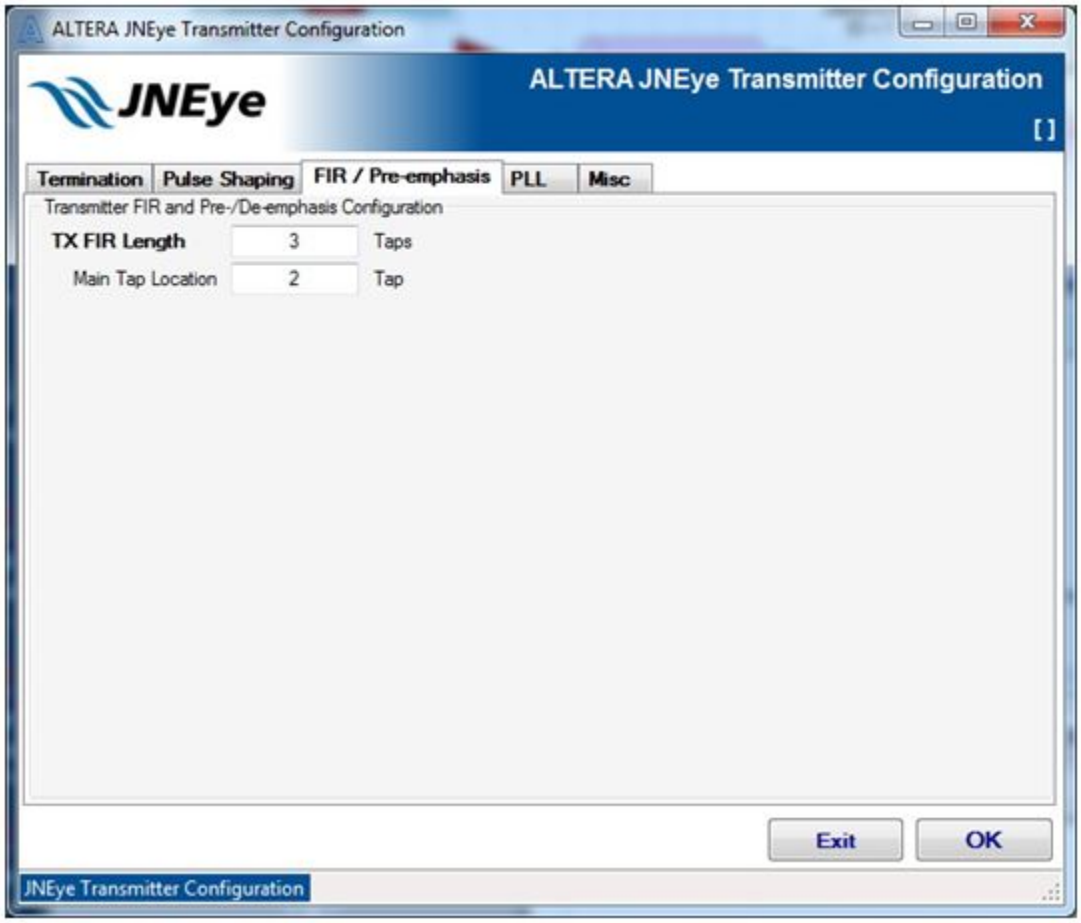
Figure 2-23: Transmitter Options: Pulse Shaping Configuration



FIR / Pre-emphasis tab

Specify the length of the TX FIR and the location of the main cursor tap. This setting is only valid for the Custom transmitter type.

Figure 2-24: Transmitter Options: Transmitter FIR, Pre-emphasis, and De-emphasis Configuration

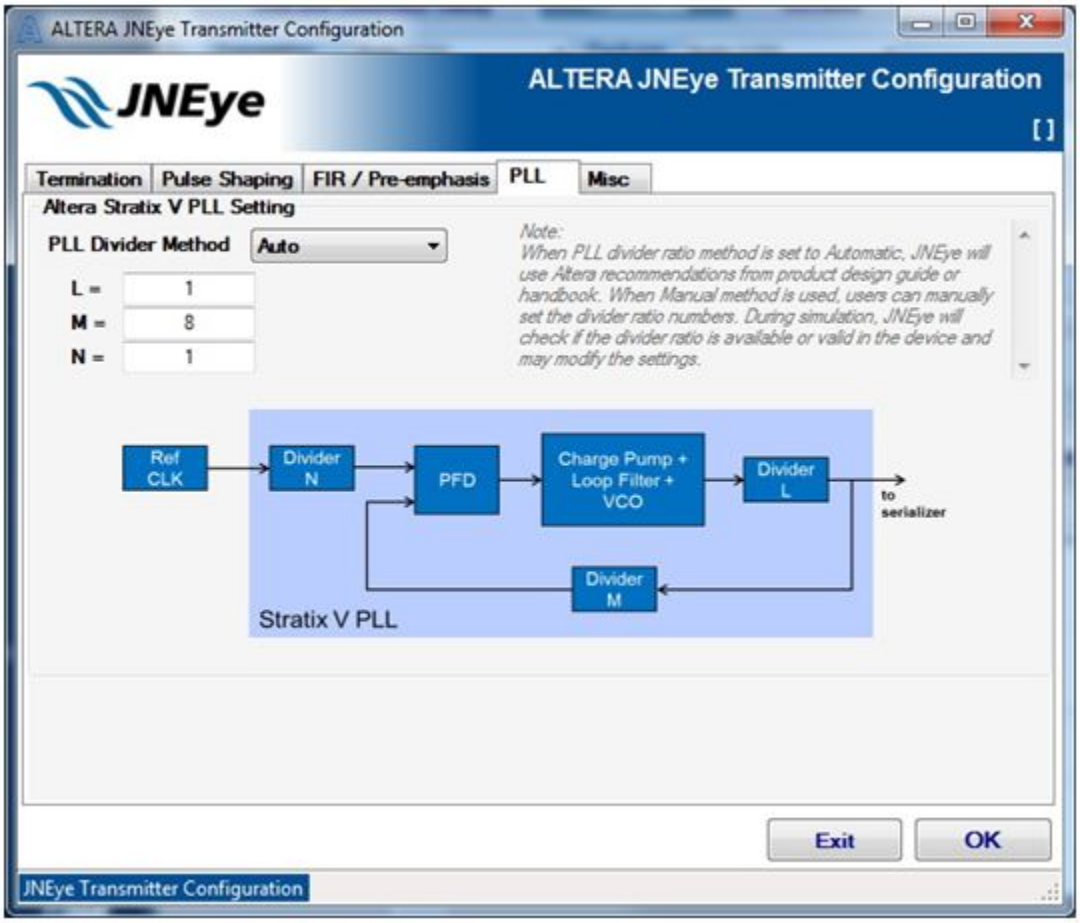


PLL tab

Use this panel to set the custom PLL divider ratio. This panel provides an alternative to JNEye's automatic divider ratio configuration. For example, Altera transmitters provide three programmable dividers: L, M, and N. You can set the divider ratio manually. Refer to Altera transceiver documentation for PLL setting recommendations.

Note: JNEye does not support the N divider.

Figure 2-25: Transmitter Options: PLL Configuration



Misc tab

Reserved. This tab is blank.

Characterization Data Access

Characterization Data Access—Transmitter jitter values can be retrieved from the built-in device characterization database.

Note: JNEye supports Arria 10 GX/SX/GT, Stratix V GT, Stratix V GX, and Arria V GZ characterization database access upon request. **If you need this capability, contact your Altera representative or supporting team for details.**

Use the following guidelines for characterization data access:

- When **Stratix V GX**, **Stratix V GT**, **Arria V GZ**, or **Arria 10 GX/SX/GT** is selected, the Characterization Data Access button appears and you can include the transmitter jitter parameters in the simulation.
- Altera Characterization Data Access covers PVT variations. You can select appropriate process, voltage, and temperature conditions that best match the desired operation conditions.
- After clicking the button, Altera Characterization Data Access configures JNEye to use the characterization data by:
  - Selecting Jitter/Noise Component Mode for characterization data entries
  - Setting the Jitter/Noise Data Lock check box
  - Importing device characterization data based on the jitter unit selection
    - **RJ**—Unit selection can be UI (RMS) or ps (RMS)
    - **Other Jitter**—Unit selection can be UI (pk-pk), UI (pk), ps (pk-pk), or ps (pk)

These actions inform the JNEye simulation engine to use the characterization data from the database.

Note:
- The characterization data is displayed in the text box for reference purposes. The JNEye simulation engine uses proprietary algorithms to accurately model the jitter and noise in the simulations.
- You can unlock the jitter and noise contents by turning off the Jitter/Noise Data Lock check box. However, the jitter and noise models and values can be different from those when the Jitter/Noise Data Lock check box is checked.
- Characterization Data Access is supported when the data rate is in the following range:
  - Stratix V GX: 5 Gbps to 14.1 Gbps
  - Stratix V GT: 19.6 Gbps to 28.1 Gbps
  - Arria V GZ: 5 Gbps to 14.1 Gbps
  - Arria V GX/SX: 3 Gbps to 17.4 Gbps (Typical PVT only)
  - Arria 10 GT: 3 Gbps to 28.3 Gbps (Typical PVT only)

  When the data rate is out of the specified range, JNEye displays a warning message and no jitter data is retrieved. If you change the data rate, you must retrieve the new jitter data by clicking **Characterization Data Access**.
- After changing the link and device configurations, such as data rate, VOD, PLL type and bandwidth, and PVT condition, you must update the jitter value by clicking **Characterization Data Access**.
- When the Jitter/Noise Data Lock check box is checked, JNEye examines whether the jitter data matches the simulation configuration during the following conditions:
  - Start simulation
  - Save link configuration
  - In batch simulation mode, jitter data is retrieved and calculated based on the link configuration

  When the link configuration exceeds the supporting range of Characterization Data Access, a warning message (conditions 1 and 2) is shown and jitter is reset (all conditions).

Figure 2-26: Characterization Data Access: PVT Conditions and Jitter/Noise Lock Check Box

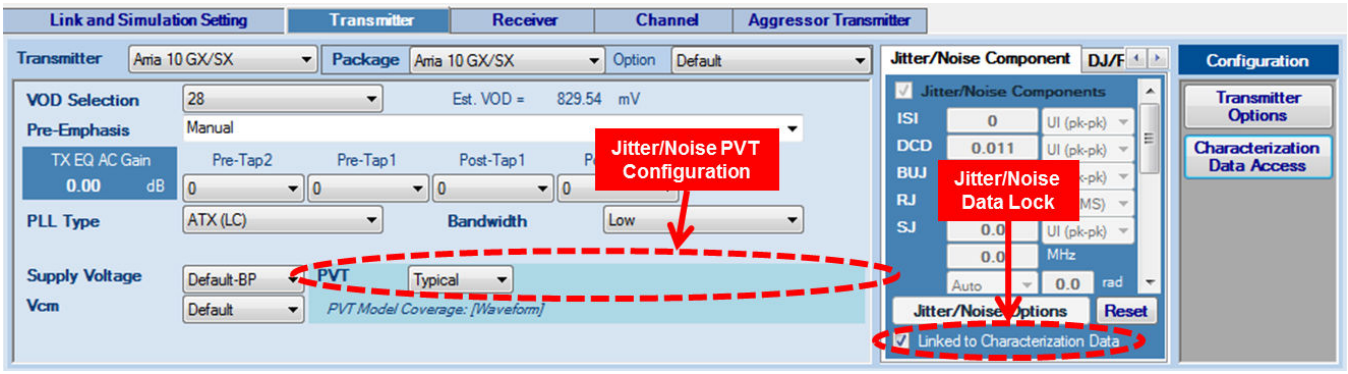
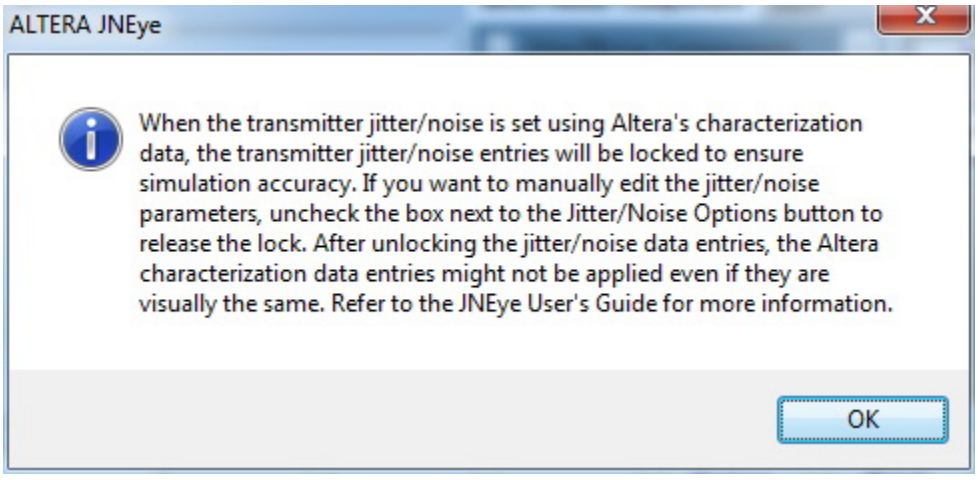
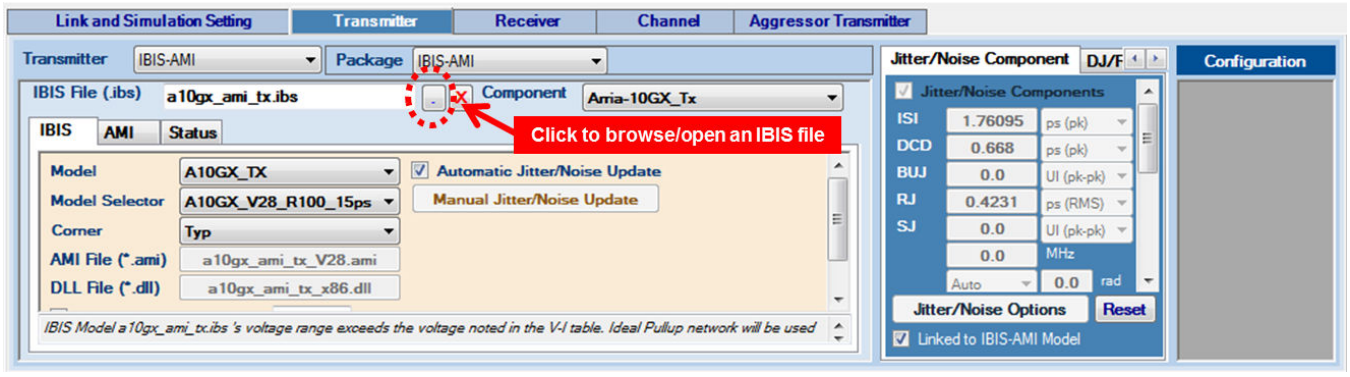


Figure 2-27: Characterization Data Access Usage and Message


ALTERA JNEye
When the transmitter jitter/noise is set using Altera's characterization data, the transmitter jitter/noise entries will be locked to ensure simulation accuracy. If you want to manually edit the jitter/noise parameters, uncheck the box next to the Jitter/Noise Options button to release the lock. After unlocking the jitter/noise data entries, the Altera characterization data entries might not be applied even if they are visually the same. Refer to the JNEye User's Guide for more information.
OK

IBIS-AMI Transmitter—JNEye supports IBIS-AMI transmitter modeling. When IBIS-AMI Transmitter is selected, the IBIS-AMI Transmitter page is shown.

Figure 2-28: Transmitter IBIS-AMI Model IBIS Configuration



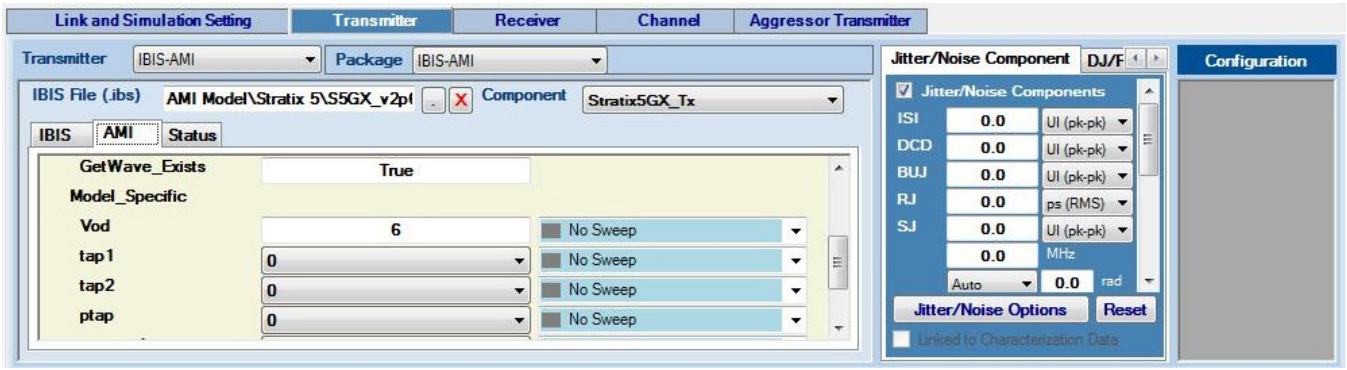
- **Package**—Package models are required in all IBIS models. JNEye includes the IBIS package model in the simulation by default. You can choose other package models by changing the Package selection to **Custom** and specifying the external package model (Channel type **Package**) as a channel component.
- **IBIS Files**—Click the file open button next to the IBIS File text box to select an IBIS model file. JNEye scans through the IBIS file and allocates all available transmitter components and models. If JNEye encounters the following issues in opening or interpreting the IBIS-AMI model, a warning message is displayed.
  - No transmitter component or model can be located.
  - The DLL for the computer platform cannot be located. The IBIS-AMI model is platform dependent. For example, a 32-bit DLL is required to simulate in a 32-bit link simulator and a 64-bit DLL is required to simulate in a 64-bit simulator. A 32-bit DLL cannot simulate in a 64-bit DLL simulator.
  - The DLL occupies too much memory and JNEye was not able to load it. However, JNEye might be able to run the simulation with such a DLL because of memory allocation differences in the JNEye GUI and the simulation engine.
- **Component**—Select an IBIS component from the IBIS model.
- **IBIS** tab—The IBIS tab shows the following configuration parameters:
  - **Model**—Select a device model within a component of an IBIS model.
  - **Model Selector**—Select a model from the model selector list.
  - **Corner**—Select the corner type of a device model. The choices are **Typ**, **Min**, and **Max**.
  - **AMI File**—Shows the AMI file specified in the IBIS model.

    Note: JNEye currently only supports device models with AMI modeling components.
  - **DLL File**—Shows the DLL file specified in the IBIS model.
  - **Use External Termination**—A checked box indicates that an external termination is used in the simulation. The external termination (single-ended) is specified in the text box on the right. The default setting is not using external termination and the default external termination (if applicable) is 50 ohms (single-ended).
  - **Use Rising/Falling Waveform**—If rising/falling waveforms are available in the IBIS model, the rising/falling waveforms are used to model the transmitter by default. If you turn off this option, ramp data (in the IBIS model) is used in the simulation.
  - **Automatic Jitter/Noise Update**—A checked box allows automatic jitter/noise updates from the IBIS-AMI model (available for models which are compliant with IBIS-AMI 6.0 and later).
  - **Manual Jitter/Noise Update**—When the **Automatic Jitter/Noise Update** option is disabled, turning on this option allows you to manually update the jitter/noise figures from the IBIS-AMI model (available for models which are compliant with IBIS-AMI 6.0 and later).

AMI tab

The AMI tab shows the following AMI configuration parameters.

Figure 2-29: Transmitter IBIS-AMI Model AMI Configuration Tab



- **Model Name**—IBIS-AMI model name

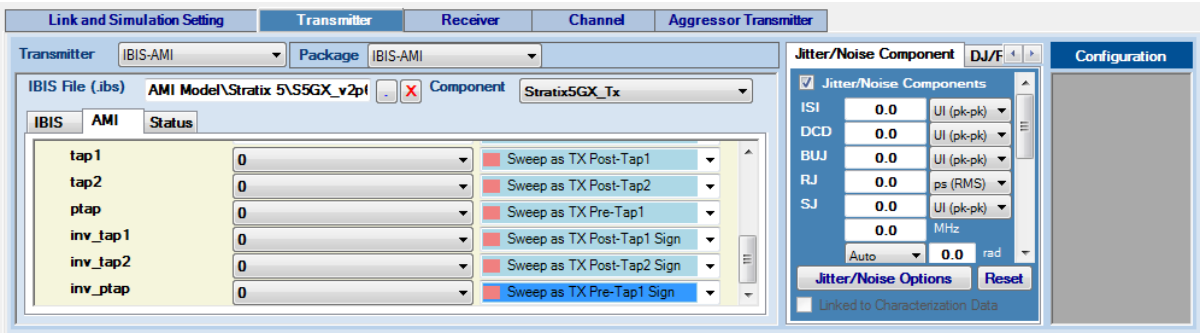
- **Reserved Parameters**:
  - The IBIS-AMI reserved parameters are shown. The reserved parameters are meant for the JNEye simulation configuration.
  - IBIS-AMI Rev 5.0 and 6.0 jitter parameters (Tx_Jitter) are extracted and automatically set in the Transmitter's Jitter/Noise window with the interpretation shown in the following table:

Table 2-9: IBIS-AMI Jitter Parameters

IBIS-AMI Tx_Jitter Parameter	JNEye Interpretation
(Tx_Jitter (Usage Info)(Type Float) (Format Gaussian <mean> <sigma>))	DJ = <mean> UI (pk) or ps (pk). Uniform distribution RJ = <sigma> UI (RMS) or ps (RMS)
(Tx_Jitter (Usage Info)(Type Float) (Format Dual-Dirac <mean> <mean> <sigma>))	DJ = (<mean> + <mean>)/2 UI (pk) or ps (pk). Dual-Dirac distribution RJ = <sigma> UI (RMS) or ps (RMS)
(Tx_Jitter (Usage Info)(Type Float) (Format DjRj < minDj > < maxDj > <sigma>))	DJ = <maxDJ> UI (pk) or ps (pk). Uniform distribution RJ = <sigma> UI (RMS) or ps (RMS)
(Tx_Jitter (Usage Info)(Type Integer Float/UI Float) (Format Table (Labels Row_No Time or UI Probability) (-5 -5e-12 1e-10) (-4 -4e-12 3e-7) …))	Refer to the transmitter jitter description in the *Jitter/Noise Component* section.
IBIS-AMI Tx_DCD Parameter	**JNEye Interpretation**
(Tx_DCD (Usage Info)(Type Float) (Format Range <typ> <min> <max>))	DCD = <typ or min or max based on corner selection> UI (pk) or ps (pk), Clock jitter distribution

- **Model Specific Parameters**—This section lists all the model specific parameters that the IBIS-AMI model provides. You can use their selections or specify parameters for the simulation.

Figure 2-30: Transmitter IBIS-AMI Parameter Type Designation for Link Optimization



JNEye 15.0 supports link optimization with IBIS-AMI transmitter models. On the left are the model specific parameters. For each parameter that JNEye determines is sweepable, a pull-down menu allows you to assign the transmitter parameters. The types of transmitter parameters are as follows:

- **No Sweep**—No sweeping or link optimization is performed
- **Sweep**—JNEye sweeps or performs link optimization using available options provided by the IBIS-AMI model
- **Sweep as TX Main Tap**—JNEye treats this parameter as the main cursor tap of transmitter equalizer in link optimization
- **Sweep as TX Main Tap Sign**—JNEye treats this parameter as the sign bit of the main cursor tap in link optimization
- **Sweep as TX Post-Tap n**—JNEye treats this parameter as the n-th post-cursor tap of transmitter equalizer in link optimization
- **Sweep as TX Post-Tap n Sign**—JNEye treats this parameter as the sign bit of the n-th post-cursor tap in link optimization
- **Sweep as TX Pre-Tap n**—JNEye treats this parameter as the n-th pre-cursor tap of transmitter equalizer in link optimization
- **Sweep as TX Pre-Tap n Sign**—JNEye treats this parameter as the sign bit of the n-th pre-cursor tap in link optimization

With the information provided in the IBIS-AMI model and parameter type selections, JNEye determines the link optimization approach and conducts the simulation. All link optimization methods are supported with IBIS-AMI transmitter models, but generally the **CTLE=>FIR=>DFE** and **CTLE=>FIR & DFE** methods are more efficient (in terms of simulation time) and effective. If you cannot determine the nature of the model specific parameters, consult with the IBIS-AMI vendors. An example of transmitter IBIS-AMI parameter type designations is shown in the above figure.

Note: As mentioned in the JNEye transmitter jitter and noise section, JNEye assumes no overlapping between jitter and noise components. Examine the IBIS-AMI Tx_Jitter parameters when they are imported into JNEye. Consult device vendors or model providers about the scope or definition of the DJ component and DCD component in the IBIS-AMI model to avoid double-counting their effects. For example, if the imported DJ already contains DCD, the DCD effect should be subtracted from the DJ figure.

Status tab

The **Status** tab shows the parameters that are fed into the IBIS-AMI model for simulations.

Figure 2-31: Transmitter IBIS-AMI Model Status Tab

Consider the following for the IBIS-AMI transmitter modeling support in JNEye:

- JNEye only supports the IBIS model with an AMI component. An IBIS model without an AMI component will not be simulated.
- Transmitter PLL is not supported when the IBIS-AMI transmitter is selected.
- JNEye supports IBIS-AMI transmitter models with the on-die S-parameter model using the **txic** IBIS-AMI keyword. When JNEye detects the **txic** keyword, the Channel Wizard helps you determine the on-die S-parameter configuration.

Related Information

Jitter/Noise Component on page 2-26

Receiver Setting

A receiver receives waveforms from the channel and processes the waveforms through the receiver equalizer and clock and data recovery module.

Figure 2-32: JNEye Receiver Settings

JNEye provides the following settings and configurations for receivers:

Receiver

The following receiver types are supported:

- Stratix V GX
- Arria V GZ
- Stratix V GT
- Arria 10 GX/SX
- Arria 10 GT
- IBIS-AMI
- Custom
- PCI Express 8GT

Parameters or selections within the receiver setting are specific to the receiver type. For example, package model, available CDR (Clock and Data Recovery) type and bandwidth, available CTLE (Continuous Time Linear Equalizer) selections, DFE operation mode and settings, and additional receiver options, are set and shown when a new device is selected. When a new receiver is chosen, it is automatically inserted into the Link Designer, ready for connecting to other link components.

Package

Select the package type for a receiver device. For Altera products and PCI-Express 8GT receivers, the package models are included in the receiver models. For Custom devices, you can specify package models in the channel setting by inserting a “Package” channel component. When you select the Custom package type (for any transmitter devices), the embedded package mode (if available) will be disabled and you can add a channel component (such as an S-parameter) with type Package in the Link Designer workspace. The Custom package model must be placed adjacent to the receiver module so it can be simulated and analyzed correctly. If you choose the Custom package type but do not add a channel component with Package type to the Link Designer workspace, the receiver is simulated without any package model.

JNEye comes with the following receiver package models:

- Stratix V GX
- Arria V GZ
- Stratix V GT
- Arria 10 GX/SX

  Options: Additional package models (shown in the following figure) are available for Arria 10 devices. The package model is specified as its trace length inside the package. These models are chosen to cover the range of package trace lengths in Arria 10 transceiver transmitters.

  - **Default**—The default package model is same as the 14 mm option
  - **14mm**
  - **16.5mm**
  - **20mm**
  - **24mm**

  Contact your Altera's representative if you would like to know how to pair your design with the Arria 10 package model options.

Figure 2-33: Arria 10 Receiver Package Options

- Arria 10 GT—Same options as Arria 10 GX/SX
- PCI-Express 8GT

CTLE Setting

Select or specify the CTLE (Continuous-Time Linear Equalizer) operation mode and model. **Auto**, **Manual**, and **Off** (if available) settings are supported.

- **Altera device receivers**:
  - Stratix V GX, Arria V GZ, Stratix V GT, Arria 10 GX/SX, and Arria 10 GT CTLE models are embedded in JNEye.
  - Both Auto and Manual settings are supported.
  - In Manual setting, EQ Bandwidth, AC Gain, and DC Gain menus are shown for user selection.
  - In Auto setting, you select the EQ bandwidth and maximum CTLE DC gain level (if available) that you want to use.
  - JNEye uses Altera's proprietary algorithm to find optimal CTLE setting in Auto setting.
- **Custom receiver and PCI-Express 8GT receiver**—You can select or input the CTLE gain (in dB) listed in the pull-down menu. The custom CTLE model uses the PCI-Express 8GT CTLE behavior model template.

Note: If you are using the Arria 10 QPI mode, manually adjust the input waveform amplitude by a constant factor of 0.4481 to get accurate QPI mode simulation results. The amplitude adjustment can be applied on the transmitter output waveform amplitude or by using an amplitude scaling channel component, such as an S-parameter, within a link. Following is an example of a 4-port constant amplitude scaling S-parameter:

```
# MHz S DB R 50.00
0.000 -400 0 -6.9725 0 -400 0 -400 0
-6.9725 0 -400 0 -400 0 -400 0
-400 0 -400 0 -400 0 -6.9725 0
-400 0 -400 0 -6.9725 0 -400 0
10.0 -400 0 -6.9725 0 -400 0 -400 0
-6.9725 0 -400 0 -400 0 -400 0
-400 0 -400 0 -400 0 -6.9725 0
-400 0 -400 0 -6.9725 0 -400 0
100.0 -400 0 -6.9725 0 -400 0 -400 0
-6.9725 0 -400 0 -400 0 -400 0
-400 0 -400 0 -400 0 -6.9725 0
-400 0 -400 0 -6.9725 0 -400 0
1000.0 -400 0 -6.9725 0 -400 0 -400 0
-6.9725 0 -400 0 -400 0 -400 0
-400 0 -400 0 -400 0 -6.9725 0
-400 0 -400 0 -6.9725 0 -400 0
10000.0 -400 0 -6.9725 0 -400 0 -400 0
-6.9725 0 -400 0 -400 0 -400 0
-400 0 -400 0 -400 0 -6.9725 0
-400 0 -400 0 -6.9725 0 -400 0
100000.0 -400 0 -6.9725 0 -400 0 -400 0
-6.9725 0 -400 0 -400 0 -400 0
-400 0 -400 0 -400 0 -6.9725 0
-400 0 -400 0 -6.9725 0 -400 0
```

VGA Bandwidth

The VGA Bandwidth selection is available when an Arria 10 GX/SX/GT model is selected. The available VGA bandwidth settings are listed in the pull-down menu. The default setting is **3** (highest bandwidth).

VGA Gain

The VGA Gain selection is available when an Arria 10 GX/SX/GT model is selected. The available VGA gain settings are listed in the pull-down menu. If **Auto** (default setting) is selected, the VGA gain setting is determined by the receiver model.

DFE Mode

The DFE can operate in **Auto mode**, **Manual mode**, or be disabled.

- **Altera receivers**:
  - Stratix V GX, Arria V GZ, Aria 10 GX/SX, and Arria 10 GT DFE models are supported in both Auto mode and Manual mode.
  - In Auto mode, JNEye finds the optimal DFE setting for the given link configuration.
  - In Manual mode, you select and set each DFE tap level.
  - For Arria 10 GX/SX/GT with floating DFE tap supports, a floating DFE tap location can be either automatically or manually set. When automatic floating DFE tap location mode is selected, JNEye uses proprietary algorithms to find the optimal floating DFE tap location.
- **Custom receiver and PCI-Express receiver**—JNEye implements a generic behavior DFE model. You can customize the DFE model with the **Receiver Options Window**.

CDR Type and CDR Bandwidth

Select the type of Clock and Data Recovery (CDR) module used in the receiver. There are two options: Ideal Clock and supported CDR type. When you select the ideal clock option, the eye diagram is plotted using the ideal system clock. When you enable CDR, both ideal clocked and CDR retimed eye diagrams are shown.

- **Altera Receivers**—Stratix V GX, Arria V GZ, Stratix V GT, Arria 10 GX/SX, and Arria 10 GT Hybrid CDR models are supported. The CDR models and configurations are automatically set according to the data rate and CDR bandwidth setting. Consult Altera design guides for CDR bandwidth configurations.
- **Custom receiver and PCI-Express 8GT receiver**—A generic CDR, with bang-bang phase detector, is supported. The CDR bandwidth for the generic receiver is 18 MHz (low bandwidth), 26 MHz (medium bandwidth), and 34 MHz (high bandwidth).

Supply Voltage

For supported devices, you can choose the supply voltage. In JNEye 15.0, the Arria 10 GX/SX/GT receiver model provides the following supply voltages:

- **Default-BP**—Supply voltage for backplane applications that have a dependency on the data rate setting
- **Default-C2C**—Supply voltage for chip-to-chip applications that have a dependency on the data rate setting
- **0.9 V** (Arria 10 GX/SX/GT)
- **1.0 V** (Arria 10 GX/SX/GT)
- **1.1 V** (Arria 10 GT)

V_{cm}

V_{cm} is the common voltage of the receiver input signal. V_{cm} options are only available when CTLE mode is QPI.

PVT

Select the process, voltage, and temperature (PVT) models for the selected receiver device. PVT model support varies depending on device type, device data availability, and model coverage. A message is shown on the Receiver tab page to indicate the PVT model coverage. Receiver PVT model coverage and conditions are shown in the following table.

Table 2-10: Receiver PVT Model Coverage

Receiver Type	Waveform PVT Model	Jitter/Noise PVT Model
Stratix V GX	Typical	Process: Typical/Fast/Slow Voltage: Typical/High/Low Temperature: –40°C to 100°C
Arria V GZ	Typical	Process: Typical/Fast/Slow Voltage: Typical/High/Low Temperature: –40°C to 100°C
Stratix V GT	Typical	Process: Typical/Fast/Slow Voltage: Typical/High/Low Temperature: 0°C to 100°C
Arria 10 GX/SX	Typical/Fast/Slow	Typical
Arria 10 GT	Typical/Fast/Slow	Typical
IBIS-AMI	Provide by IBIS-AMI model	Provide by IBIS-AMI model
Custom	None	None
PCI-Express 8GT	None	None

JNEye to Quartus II Parameter Translation for Arria 10 GX/SX/GT Receivers

The following table shows the mapping between the JNEye's Arria 10 GX/SX/GT receiver model parameters and the **Assignments Editor** entries in the Quartus II software. Unless otherwise noted, values translate directly between the two domains.

Table 2-11: JNEye to Quartus II Parameter Translation for Arria 10 GX/SX/GT Receivers

JNEye Name	Quartus II Name
Receiver Options > **Termination** > **R**	Receiver On-Chip- Termination
Supply Voltage	Vccer/Vccet Power

JNEye Name	Quartus II Name
CTLE Setting / Mode	Eq_bw_sel (Equalizer bandwidth Selection) If Receiver High Data Rate Mode Equalizer = 1 • 0: JNEye CTLE Setting / Mode = High Data Rate, Peak Freq 0 • 1: JNEye CTLE Setting / Mode = High Data Rate, Peak Freq 1 • 2: JNEye CTLE Setting / Mode = High Data Rate, Peak Freq 2 • 3: JNEye CTLE Setting / Mode = High Data Rate, Peak Freq 3 If Receiver High Data Rate Mode Equalizer = 0 • 0: JNEye CTLE Setting / Mode = High Gain, Low BW • 1: JNEye CTLE Setting / Mode = High Gain, High BW
VGA BW	VGA_bandwidth_Select
CTLE Setting / Mode	Receiver High Data Rate Mode Equalizer If Receiver High Data Rate Mode Equalizer = 1 • JNEye CTLE Setting / Mode = High Data Rate If Receiver High Data Rate Mode Equalizer = 0 • JNEye CTLE Setting / Mode = High Gain
CTLE Setting • Auto • Manual	Refer to the *Arria 10 Transceiver PHY User Guide*
AC Gain with CTLE Setting = Manual Mode = High Data Rate	Receiver High Data Rate Mode Equalizer AC Gain Control
AC Gain with CTLE Setting = Manual Mode = High Gain	Receiver High Gain Mode Equalizer AC Gain Control
DC Gain with CTLE Setting = Manual Mode = High Gain	Receiver High Gain Mode Equalizer DC Gain Control
VGA Gain	Receiver Variable Gain Amplifier Voltage Swing Select
DFE Mode	Receiver Decision Feedback Equalizer Mode
DFE Tap 1	Receiver Decision Feedback Equalizer Fix Tap One Coefficient

JNEye Name	Quartus II Name
DFE Tap 2	Receiver Decision Feedback Equalizer Fix Tap Two Coefficient
DFE Tap 3	Receiver Decision Feedback Equalizer Fix Tap Three Coefficient
DFE Tap 4	Receiver Decision Feedback Equalizer Fix Tap Four Coefficient
DFE Tap 5	Receiver Decision Feedback Equalizer Fix Tap Five Coefficient
DFE Tap 6	Receiver Decision Feedback Equalizer Fix Tap Six Coefficient
DFE Tap 7	Receiver Decision Feedback Equalizer Fix Tap Seven Coefficient
RX Impedance (R in Receiver Options / Termination)	Receiver On-Chip- Termination
CDR Type Hybrid	Arria 10 Transceiver CMU PLL
CDR Bandwidth	Bandwidth in PLL Options

Jitter/Noise Setting

JNEye provides extensive jitter and noise modeling and configuration capabilities. The receiver intrinsic jitter and noise types are categorized in the following table. You can configure each jitter and noise type by clicking **Receiver Jitter Options**, which leads to the Receiver Jitter/Noise Configuration window.

JNEye uses a flat jitter/noise structure that assumes no overlapping among the jitter and noise components. Avoid double counting when inputting or importing jitter/noise figures. In the following figure, DJ contains DCD, ISI, PJ, and BUJ. This implies that when you specify DCD and BUJ, the DJ should not be used or the DJ figure should not contain any DCD and BUJ components.

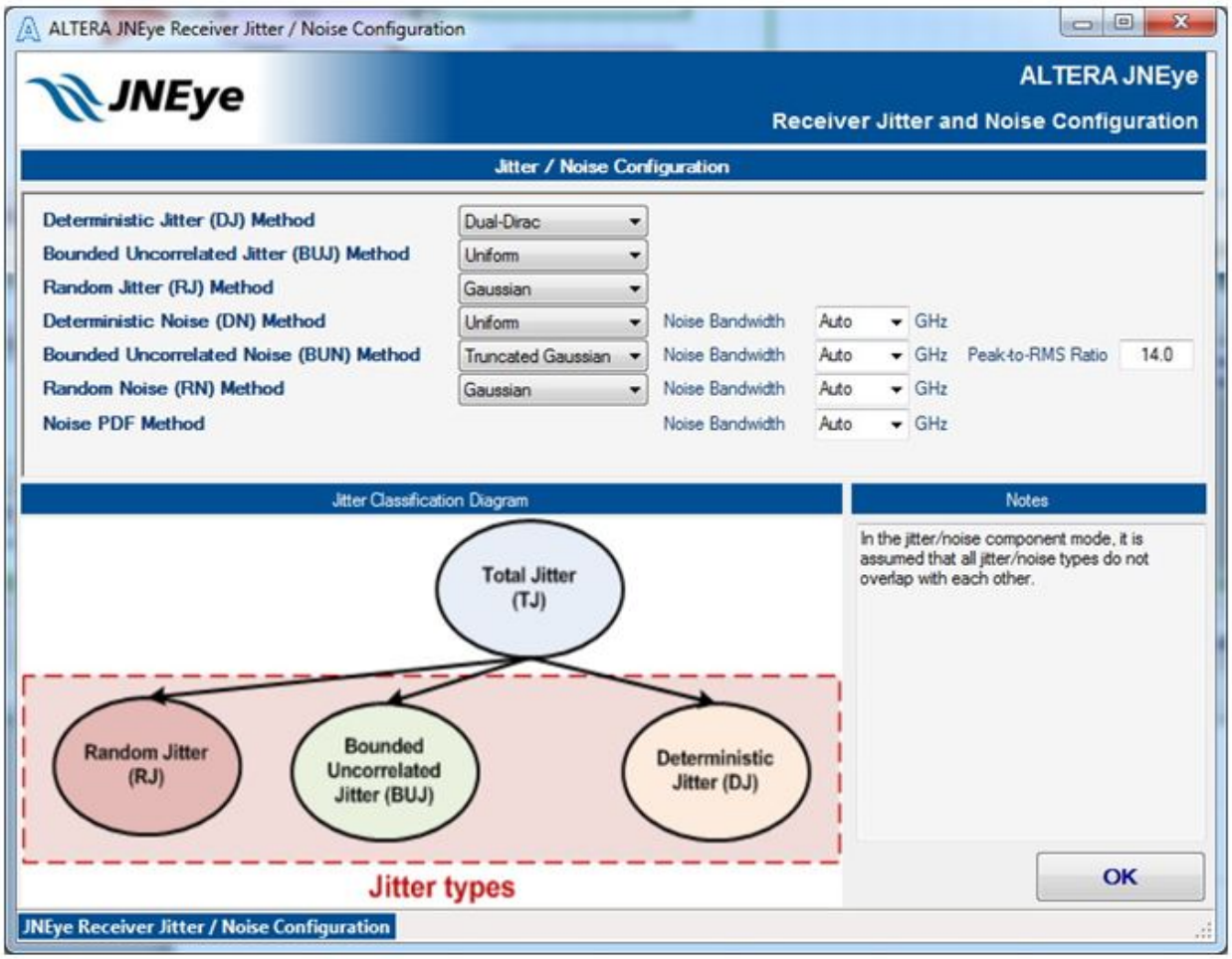
Table 2-12: Receiver Intrinsic Jitter and Noise Types

Name	Description	Unit	Support in JNEye	Comments
DJ	Deterministic Jitter	UI	Yes	You can generate the receiver DJ by using a uniform distribution, dual-Dirac, or truncated Gaussian method. You can select the DJ generation method in the **Receiver Jitter/Noise Configuration Window**. The default receiver DJ method is dual-Dirac.

Name	Description	Unit	Support in JNEye	Comments
BUJ	Bounded Uncorrelated Jitter	UI	Yes	Same as receiver's Deterministic Jitter. The default method is Uniform distribution. You can select the BUJ generation method in the **Receiver Jitter/Noise Configuration Window**.
RJ	Random Jitter	UI-RMS or ps-RMS	Yes	RJ is assumed to be Gaussian. You can specify the receiver RJ in eighth pico-second (ps-RMS) or unit-interval (UI-RMS).
DN	Deterministic Noise	mV	Yes	You can generate the receiver DN by using a uniform distribution, dual-Dirac, or truncated Gaussian method. You can select the DN generation method in the **Receiver Jitter/Noise Configuration Window**. The default DJ method is uniform.
BUN	Bound Uncorrelated Noise	mV	Yes	Same as receiver DN above. The default method is Truncated Gaussian method. You can select the BUN generation method in the **Receiver Jitter/Noise Configuration Window**.
RN	Random Noise	mV-RMS	Yes	RN is assumed to be Gaussian.
Jitter PDF	Jitter Probability Density Function (PDF)	Jitter amplitude, Probability (Jitter amplitude can be in absolute time or UI (unit interval) unit)	Yes	Jitter PDF defines the jitter probability density function. The input format is jitter amplitude in second and probability. The following is a jitter PDF example: -5e-12 1e-10 -4e-12 3e-7 -3e-12 1e-4 -2e-12 1e-2 -1e-12 0.29 0 0.4 1e-12 0.29 2e-12 1e-2 3e-12 1e-4 4e-12 3e-7 5e-12 1e-10

Name	Description	Unit	Support in JNEye	Comments
Noise PDF	Noise Probability Density Function	Noise amplitude, Probability	Yes	Noise PDF defines the noise probability density function. The input format is Noise amplitude in volt and probability. The following is a noise PDF example: -50e-3 1e-10 -40e-3 3e-7 -30e-3 1e-4 -20e-3 1e-2 -10e-3 0.29 0 0.4 10e-3 0.29 20e-3 1e-2 30e-3 1e-4 40e-3 3e-7 50e-3 1e-10

Figure 2-34: JNEye Receiver Jitter/Noise Configuration Window



Characterization Data Access

You can retrieve the receiver jitter values from the built-in device characterization database. JNEye supports Arria 10 GX/SX/GT, Stratix V GT, Stratix V GX, and Arria V GZ characterization database access upon request. **If you need this capability, contact your Altera representative or supporting team for details.**

Use the following guidelines for characterization data access:

- When **Stratix V GX**, **Stratix V GT**, **Arria V GZ**, or **Arria 10 GX/SX/GT** is selected, the **Characterization Data Access** button appears and you can include the receiver jitter parameters in the simulation.
- Characterization Data Access covers PVT variations. You can select the appropriate process, voltage, and temperature conditions that best match the desired operation conditions.
- After clicking **Characterization Data Access**, JNEye is configured to use the characterization data by:
  - Setting Jitter/Noise Component Mode for characterization data entries
  - Setting the Jitter/Noise Data Lock check box
  - Importing device characterization data based on the jitter unit selection
    - **RJ**—Unit selection can be UI (RMS) or ps (RMS)
    - **Other Jitter**—Unit selection can be UI (pk-pk), UI (pk), ps (pk-pk), or ps (pk)

The JNEye simulation engine uses this characterization data from the database.

Note:
- The characterization data is displayed in the text box for reference purposes. The JNEye simulation engine uses proprietary algorithms to accurately model the jitter and noise in the simulations.
- You can unlock the jitter and noise contents by turning off the Jitter/Noise Data Lock check box. However, the jitter and noise models and values can be different from those when the Jitter/Noise Data Lock check box is checked.
- Characterization Data Access is supported when the data rate is in the following range:
  - Stratix V GX: 5 Gbps to 14.1 Gbps
  - Stratix V GT: 19.6 Gbps to 28.1 Gbps
  - Arria V GZ: 5 Gbps to 14.1 Gbps
  - Arria V GX/SX: 3 Gbps to 17.4 Gbps
  - Arria 10 GT: 3 Gbps to 28.3 Gbps

  When the data rate is out of the specified range, JNEye displays a warning message and no jitter data is retrieved. If you change the data rate, you must retrieve the new jitter data by clicking **Characterization Data Access**.
- After changing the link and device configurations, such as data rate, bandwidth, and PVT condition, you must update the jitter value by clicking **Characterization Data Access**.
- When the Jitter/Noise Data Lock check box is checked, JNEye examines whether the jitter data matches the simulation configuration during the following conditions:
  - Start simulation
  - Save link configuration
  - In batch simulation mode, jitter data is retrieved and calculated based on the link configuration

  When the link configuration exceeds the supporting range of Characterization Data Access, a warning message (conditions 1 and 2) is shown and jitter is reset (all conditions).

Figure 2-35: Characterization Data Access: PVT Conditions and Jitter/Noise Lock Check Box

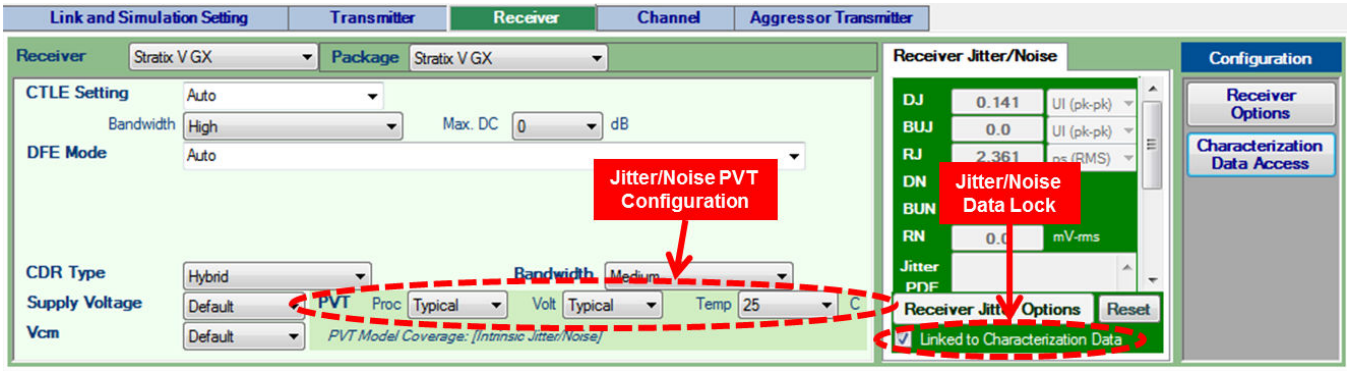
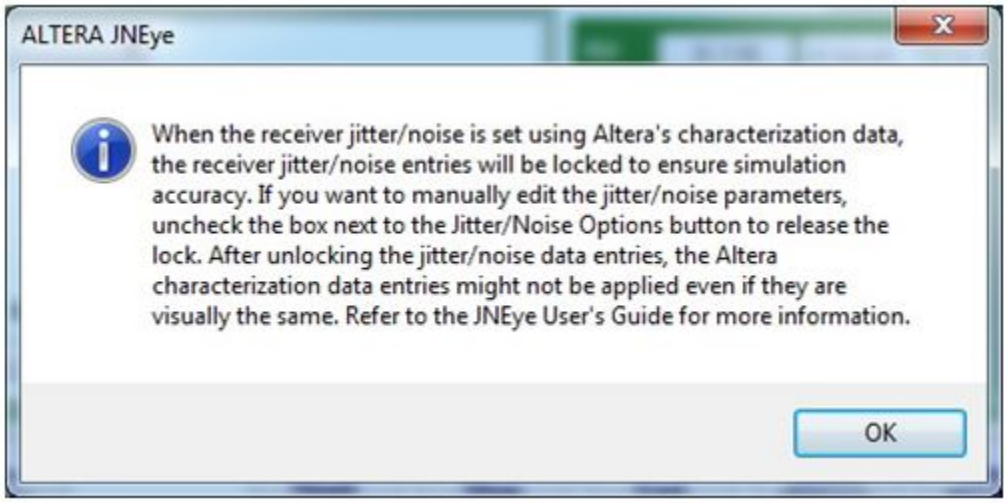


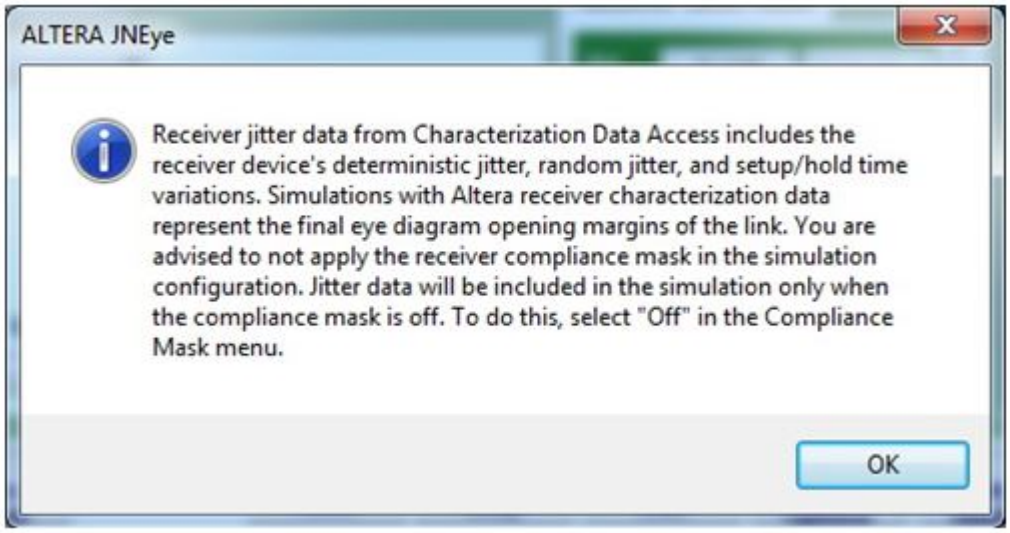
Figure 2-36: Characterization Data Access Usage and Message


ALTERA JNEye
When the receiver jitter/noise is set using Altera's characterization data, the receiver jitter/noise entries will be locked to ensure simulation accuracy. If you want to manually edit the jitter/noise parameters, uncheck the box next to the Jitter/Noise Options button to release the lock. After unlocking the jitter/noise data entries, the Altera characterization data entries might not be applied even if they are visually the same. Refer to the JNEye User's Guide for more information.
OK

A message box appears when the Characterization Data Access button is clicked.

Note: The characterization data is only included in the simulation when the compliance mask is disabled (set to **Off**). Refer to the Compliance Mask section for references.

Figure 2-37: Altera Receivers Jitter Data Usage Message Window

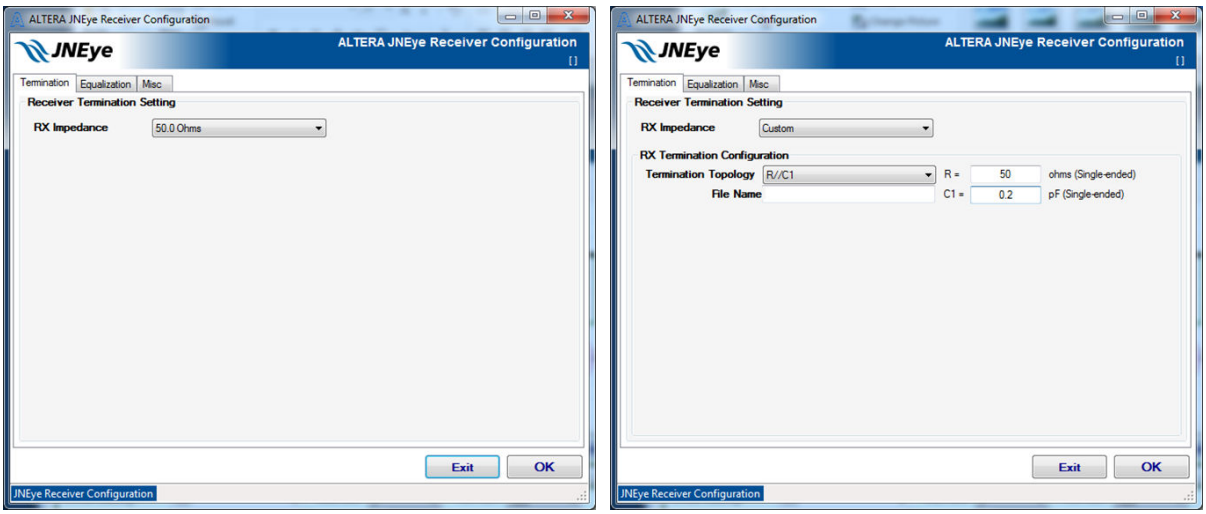

ALTERA JNEye
Receiver jitter data from Characterization Data Access includes the receiver device's deterministic jitter, random jitter, and setup/hold time variations. Simulations with Altera receiver characterization data represent the final eye diagram opening margins of the link. You are advised to not apply the receiver compliance mask in the simulation configuration. Jitter data will be included in the simulation only when the compliance mask is off. To do this, select "Off" in the Compliance Mask menu.
OK

Receiver Options

Receiver options provide further configuration and setting options for receivers.

- **Termination** tab—This section specifies receiver impedance.

Figure 2-38: Receiver Termination Configuration



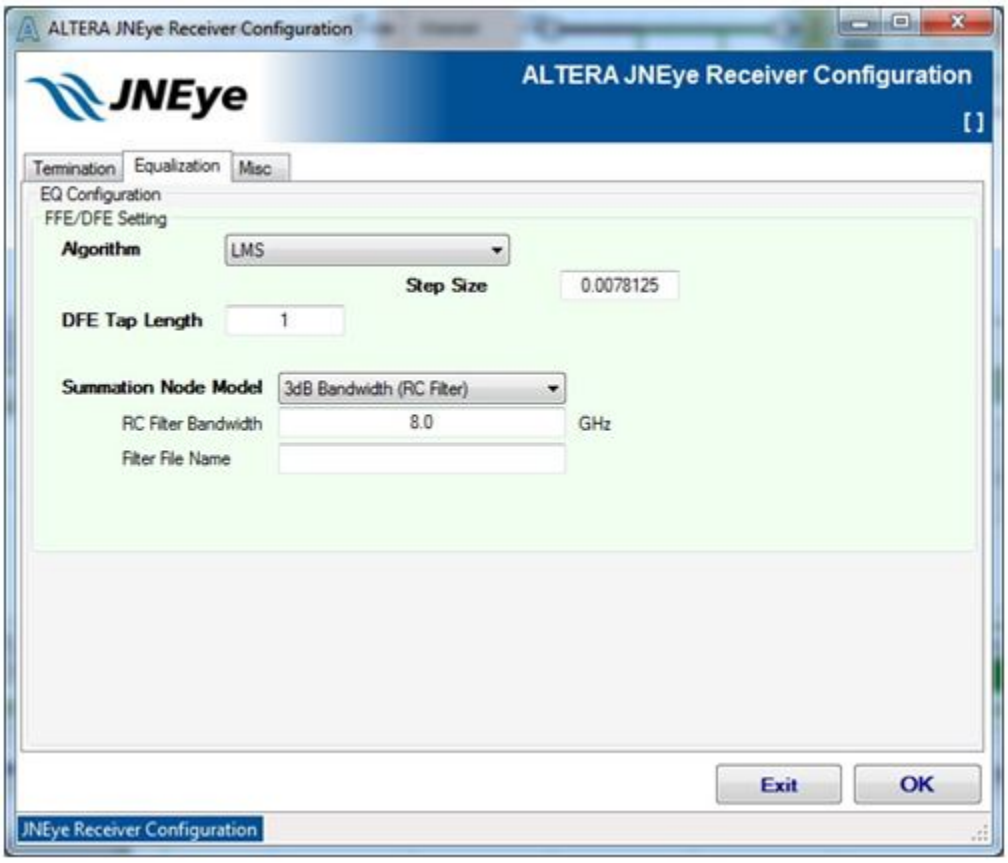
For selected Altera devices, use the **RX Impedance** pull-down menu to select a termination configuration. You can also customize the termination configuration by selecting the **Custom** option. When the **Custom** RX Impedance method is chosen, the termination can be configured as follows:

- **Ideal** TX termination—The transmitter is ideal with a 50 ohms (single-ended) termination.
- **Non-ideal** TX termination—Select one of the following options:
  - **R**—Transmitter impedance is modeled as a resistance R ohms (single-ended).
  - **R//C1**—Transmitter impedance is modeled as an RC network with a parallel resistor (in ohms) and a capacitance (in pF).
  - **File Input** (Frequency Real Imaginary)—Transmitter impedance is modeled by a frequency-dependent complex impedance table described in the input file.

For an Altera transmitter, the default termination configurations are automatically selected and specified.

- **Equalization** tab—For Arria 10 GX/SX/GT, Stratix V GX, and Arria V GZ devices, the DFE model is embedded in the JNEye and is not configurable. For Custom and PCI-Express 8GT receivers, the following options are provided.

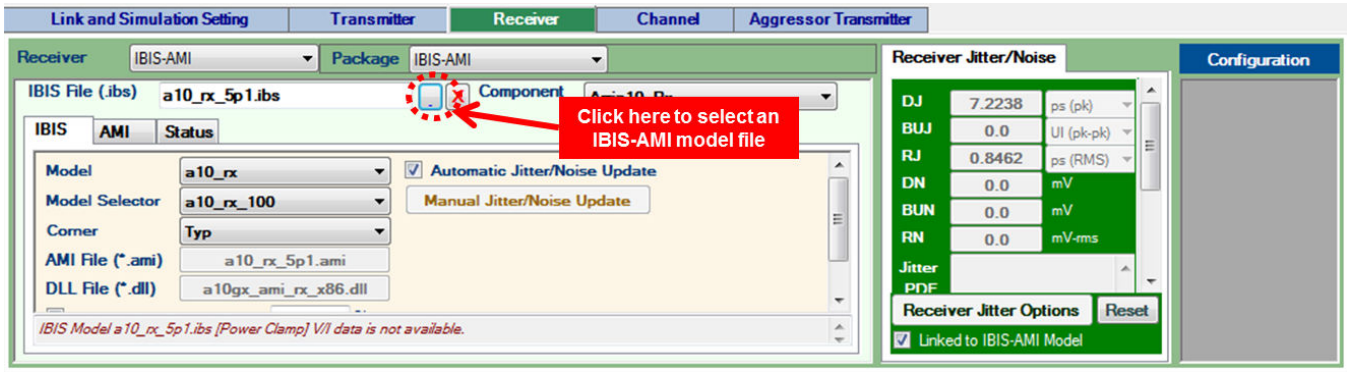
Figure 2-39: JNEye Receiver Options: Equalization Configuration



- **Algorithm**—The DFE is adapted using the LMS algorithm and its variations.
- **Step Size**—Step size of the LMS algorithm. This parameter controls the speed of the LMS adaptation. The default value is 0.01.
- **DFE Tap Length**—Number of DFE taps. This option is only available for Custom and PCI-Express 8GT receivers.
- **Summation Node Model**—JNEye supports two generic/custom summation node modeling methods:
  - **3dB Bandwidth (RC filter)**—Use a first-order RC filter to perform low-pass filtering of the DFE adjustment.
  - **S-parameter**—Use your S-parameter file to specify a pulse-shaping filter. Only the differential insertion loss (S_{dd21}) is applied in the pulse shaping.
- **Misc** tab—Reserved. This tab is blank.

IBIS-AMI Receiver—JNEye supports IBIS-AMI receiver modeling. When you select the IBIS-AMI receiver, the IBIS-AMI Receiver page appears. The IBIS-AMI page includes three tabs for additional settings of the IBIS-AMI model.

Figure 2-40: Receiver IBIS-AMI Model IBIS Configuration Page



- **Package**—Package models are required in all IBIS models. JNEye includes the IBIS package model in the simulation by default. You can choose other package models by changing the Package selection to **Custom** and specifying the external package model (Channel type **Package**) as a channel component.
- **IBIS Files**—Click the file open button next to the IBIS File text box to select an IBIS model file. JNEye scans through the IBIS file and allocates all available receiver components and models. If JNEye encounters any of the following issues in opening or interpreting the IBIS-AMI model, a warning message will be shown.
  - No receiver component or model can be located.
  - The DLL for the computer platform cannot be located. Note that the IBIS-AMI model is platform dependent. For example, a 32-bit DLL is required to simulate in a 32-bit link simulator. A 64-bit DLL is required to simulate in a 64-bit simulator. A 32-bit DLL cannot simulate with a 64-bit DLL in the same simulation.
  - The DLL occupies so much memory that JNEye was not able to load it. However, JNEye might be able to run the simulation with such a DLL because of memory allocation differences in the JNEye GUI and the simulation engine.
- **Component**—Select an IBIS component from the IBIS model.

IBIS tab

- **Model**—Select a device model within a component of an IBIS model.
- **Model Selector**—Select a model from the model selector list.
- **Corner**—Select the corner type of a device model. The choices are **Typ**, **Min**, and **Max**.
- **AMI File**—Shows the AMI file specified in the IBIS model.

  Note: JNEye currently only supports device models with AMI modeling components.
- **DLL File**—Shows the DLL file specified in the IBIS model.

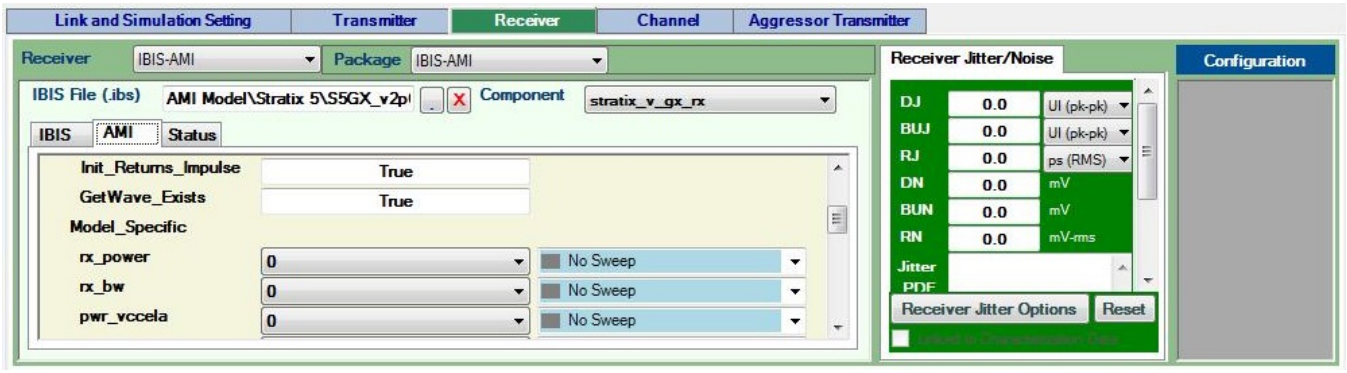
- **Use External Termination**—A checked box indicates that an external termination is used in the simulation. The external termination (single-ended) is specified in the text box on the right. The default setting is not using external termination and the default external termination (if applicable) is 50 ohms (single-ended).

  Note: JNEye automatically enables the external termination option when it detects that the IBIS-AMI model is using [series pin mapping] with [R series] configuration.
- **Automatic Jitter/Noise Update**—A checked box allows automatic jitter/noise updates from the IBIS-AMI model (available for models which are compliant with IBIS-AMI 6.0 and later).
- **Manual Jitter/Noise Update**—When the **Automatic Jitter/Noise Update** option is disabled, turning on this option allows you to manually update the jitter/noise figures from the IBIS-AMI model (available for models which are compliant with IBIS-AMI 6.0 and later).

AMI tab

The AMI tab shows the following AMI configuration parameters.

Figure 2-41: Receiver IBIS-AMI Model AMI Configuration Tab



- **Model Name**—IBIS-AMI model name
- **Reserved Parameters**:
  - The IBIS-AMI reserved parameters are shown. The reserved parameters are meant for the JNEye simulation configuration.
  - JNEye supports the IBIS-AMI Rev. 5.0 and 6.0 jitter format. IBIS-AMI receiver jitter parameters (Rx_Clock_PDF) are extracted and automatically set in the Receiver's Jitter/Noise window with the interpretation shown in the following table:

Table 2-13: IBIS-AMI Receiver Jitter Parameters

IBIS-AMI Rx_Clock_PDF Parameter	JNEye Interpretation
(Rx_Clock_PDF (Usage Info)(Type Float) (Format Gaussian <mean> <sigma>))	DJ = <mean> UI (pk) or ps (pk), Uniform distribution RJ = <sigma> UI (RMS) or ps (RMS)
(Rx_Clock_PDF (Usage Info)(Type Float) (Format Dual-Dirac <mean> <mean> <sigma>))	DJ = (<mean> + <mean>)/2 UI (pk) or ps (pk), Dual-dirac distribution RJ = <sigma> UI (RMS) or ps (RMS)
(Rx_Clock_PDF (Usage Info)(Type Float) (Format DjRj < minDj > < maxDj > <sigma>))	DJ = <maxDJ> UI (pk) or ps (pk), Uniform distribution RJ = <sigma> UI (RMS) or ps (RMS)
(Rx_Clock_PDF (Usage Info)(Type Integer Float/UI Float) (Format Table (Labels Row_No Time or UI Probability) (-5 -5e-12 1e-10) (- 4 - 4e-12 3e-7) …))	Refer to receiver jitter PDF
IBIS-AMI RX_Receiver_Sensitivity Parameter	**JNEye Interpretation**
(Rx_Receiver_Sensitivity (Usage Info)(Type Float) (Format Value <value>))	Not supported
(Rx_Receiver_Sensitivity (Usage Info)(Type Float) (Format Range < typ > <min> <max>))	Not supported
(Rx_Receiver_Sensitivity (Usage Info)(Type Float) (Format Corner <slow> <fast>))	Not supported

- **Model Specific Parameters**— This section lists all the model specific parameters that the IBIS-AMI model provides. You can use their selections or specify parameters for the simulation.

Figure 2-42: Receiver IBIS-AMI Parameter Type Designation for Link Optimization

JNEye 15.0 supports link optimization with IBIS-AMI receiver models. On the left are the model specific parameters. For each parameter that JNEye determines is tunable, a pull-down menu allows you to assign the receiver parameters. The types of receiver parameters are as follows:

- **No Sweep**—No sweeping or link optimization is performed
- **Sweep**—JNEye sweeps or performs link optimization using available options provided by the IBIS-AMI model. This parameter is not supported in the JNEye 15.0 release.
- **CTLE Adapt Controller**—This receiver parameter enables or disables automatic adaptation of the CTLE or analog equalizer. This sweep parameter is used when the link optimization method is **CTLE=>FIR=>DFE** or **CTLE=>FIR & DFE**.
- **DFE Adapt Controller**—This receiver parameter enables or disables automatic adaptation of the DFE. This sweep parameter is used when the link optimization method is **CTLE=>FIR=>DFE** or **CTLE=>FIR & DFE**.
- **Sweep as CTLE**—This receiver parameter is swept as the CTLE or analog equalizer with all available options.
- **Sweep as CTLE AC Gain**—Tthis receiver parameter is swept as the CTLE's AC gain controller. This sweep parameter is generally used in conjunction with the **Sweep as CTLE DC Gain** parameter.
- **Sweep as CTLE DC Gain**—This receiver parameter is swept as the CTLE's DC gain controller. This sweep parameter is generally used in conjunction with the **Sweep as CTLE AC Gain** parameter.

With the information provided in the IBIS-AMI model and parameter type selections, JNEye determines the link optimization approach and conducts the simulation. If you cannot determine the nature of the model specific parameters, consult with the IBIS-AMI vendors. An example of transmitter IBIS-AMI parameter type designations is shown in the above figure.

Note: JNEye assumes no overlapping between jitter and noise components. Examine the IBIS-AMI Rx_Clock_PDF parameters when they are imported into JNEye. Consult device vendors or model providers about the scope or definition of the DJ component and DCD component in the IBIS-AMI model to avoid double-counting their effects.

Status tab

The Status tab shows the parameters that are fed into the IBIS-AMI model for simulations.

Figure 2-43: Receiver IBIS-AMI Model Status Tab

Note: Consider the following for the IBIS-AMI receiver modeling support in JNEye:

- JNEye only supports the IBIS model with an AMI component. An IBIS model without an AMI component will not be simulated.
- Rx_Receiver_Sensitivity is not supported in this JNEye release
- Receiver CDR is supported by the IBIS-AMI model itself
- JNEye supports IBIS-AMI receiver models with the on-die S-parameter model using the **rxic** IBIS-AMI keyword. When JNEye detects the **rxic** keyword, the Channel Wizard helps you determine the on-die S-parameter configuration.

Channel Setting

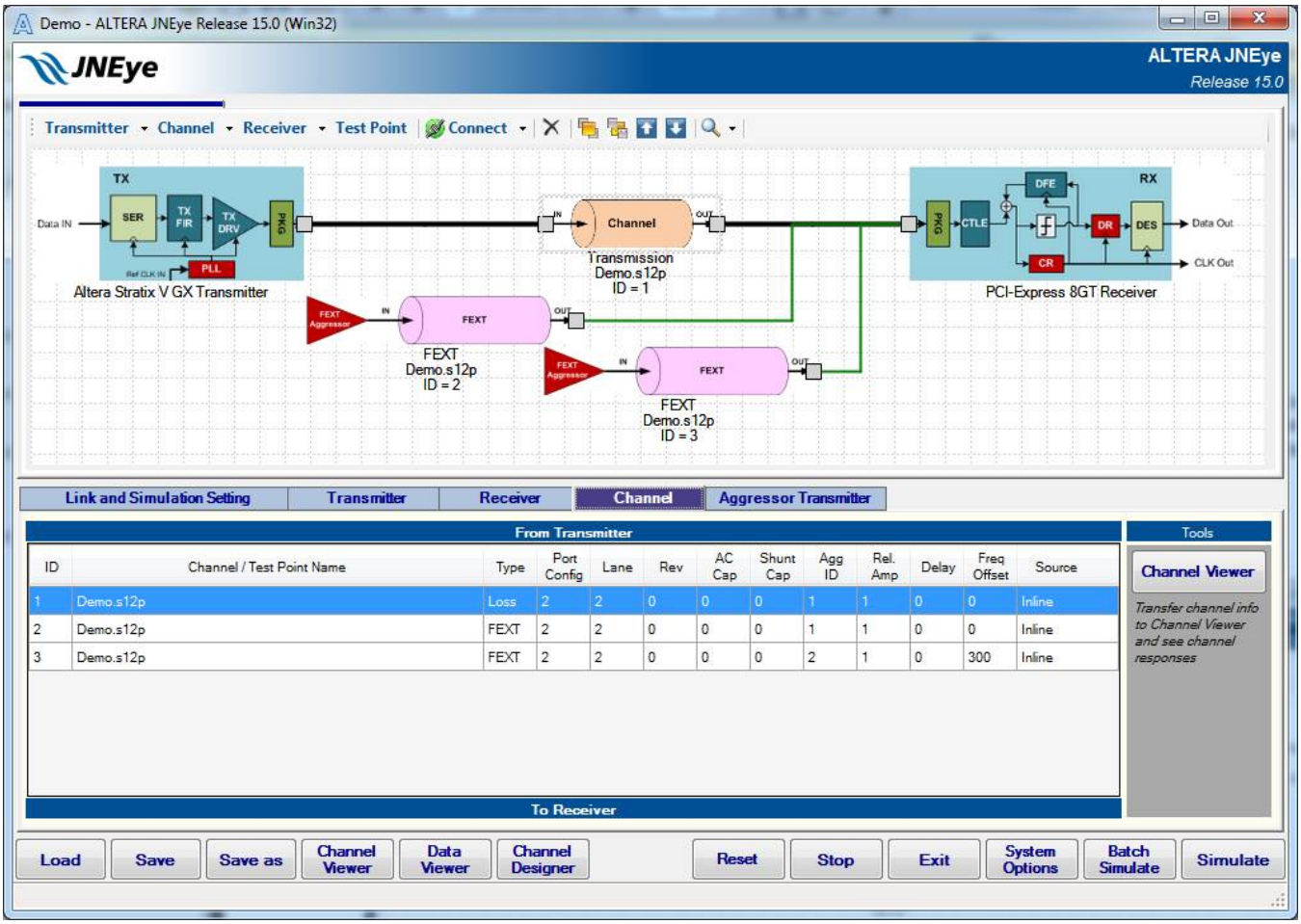
The channel connects the transmitter and the receiver. It contains transmission media such as PCB traces, connectors, backplanes, cables, and device packages. A channel is a combination of numerous components described by channel models. JNEye's channel processing engine first interprets the channel models and then cascades channels to construct one channel component for link simulations.

JNEye supports **single-ended Touchstone S-parameter** channel models. It can access and process *n-port* S-parameters and extract transmission responses and crosstalk responses. After successfully extracting the channel characteristics, it performs differential-pair channel cascading for subsequent link simulation.

Note: Make sure the single-ended Touchstone S-parameter is used in JNEye. Unexpected results will be seen if you use a mixed-mode (or differential-mode) S-parameter in a simulation. If you receive a mixed-mode S-parameter file, Altera recommends you convert it to single-ended format using third-party tools. Consult your Altera supporting team if you have questions about this subject.

JNEye implements the Link Designer, which allows you to graphically construct the communication link. In the following figure, the Channel List shows the channel construction example with one transmission channel (such as a loss channel or a victim channel) and two crosstalk channels.

Figure 2-44: JNEye Channel Setting with Link Design and Channel List



An S-parameter channel component such as a connector, cable, or backplane can be described by the following parameters or information:

- **ID**—Sequence or location of the channel component. The top channel is connected to the transmitter and the bottom channel is connected to the receiver.

  Note: Embedded package models (such as Package models for Altera devices and PCI Express Gen3 devices) are not shown in the channel list or Link Designer.
- **Channel Name**—An S-parameter file that describes the channel component. The S-parameter can be 4-port, 8-port, 12-port, 16-port, and so forth. When your cursor hovers on a channel list, a tooltip shows the S-parameter file location. This information is useful if you share JNEye configuration files.
- **Type**—Specify the type of channel characteristics to be used in the link simulation. The type of channel characteristics can be insertion loss (**Loss**), far-end crosstalk (**FEXT**), or near-end crosstalk (**NEXT**). You can change the channel (or channel type) by selecting the channel from the Link Designer using the Channel Wizard.
- **Port Configuration**—Depending on the S-parameter measurement condition, the port configuration can be one of the following types. Use the **Channel Wizard** to change the port configuration of an S-parameter.

Figure 2-45: S-parameter with Port Configuration – Type 1

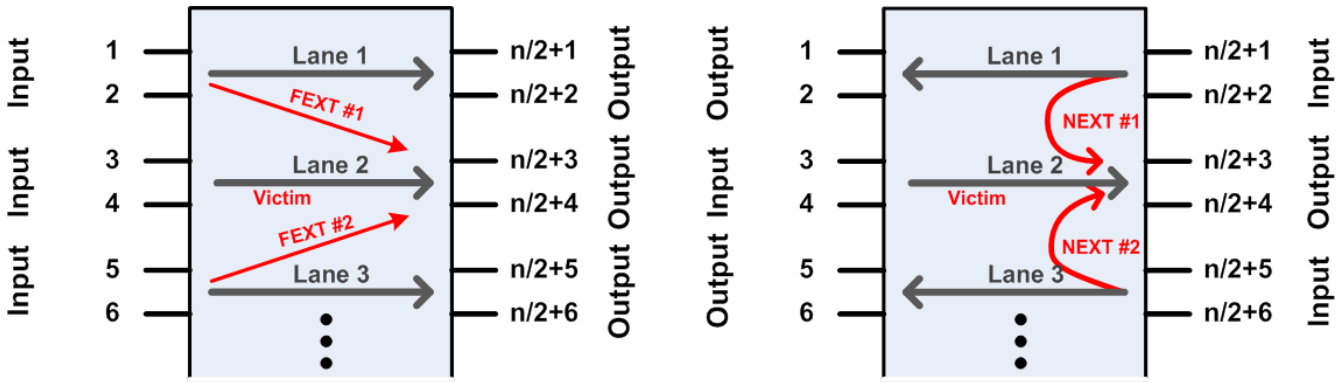


Figure 2-46: S-parameter with Port Configuration – Type 2

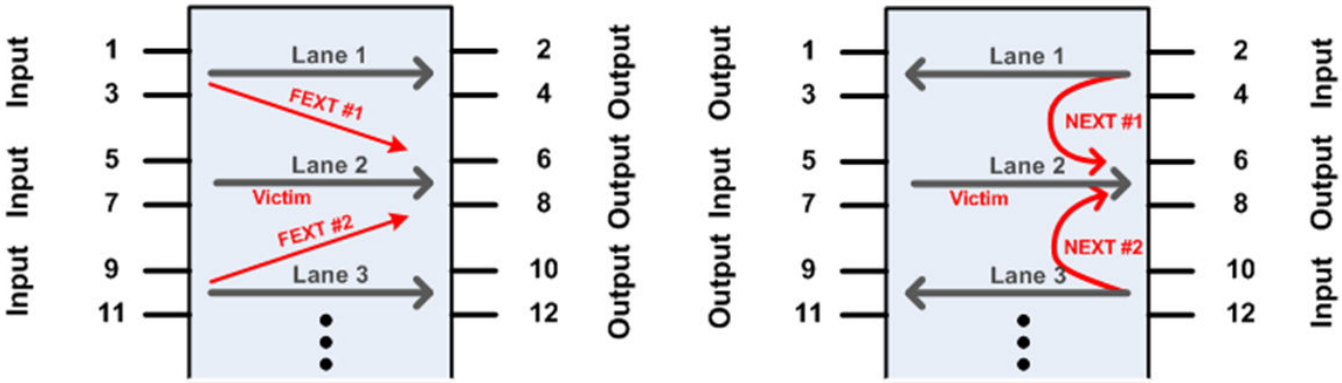


Figure 2-47: S-parameter with Port Configuration – Type 3

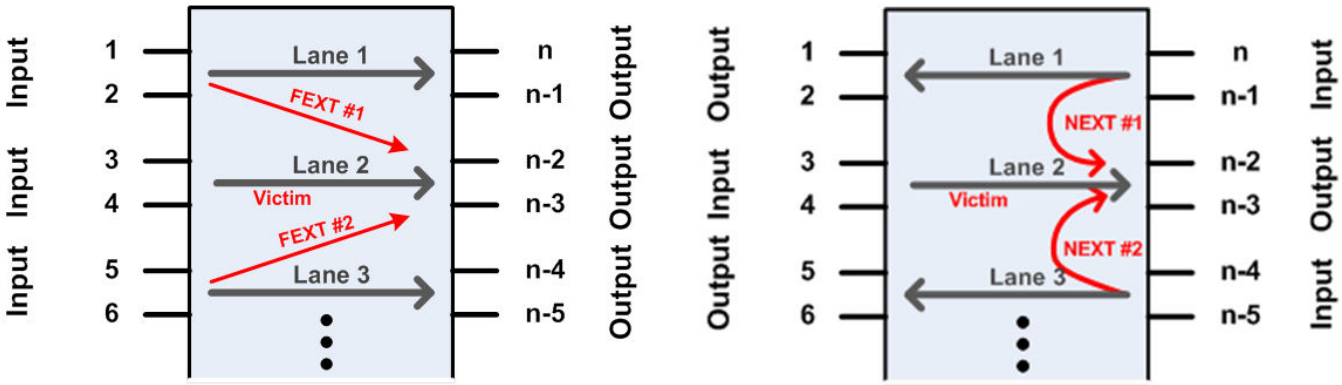
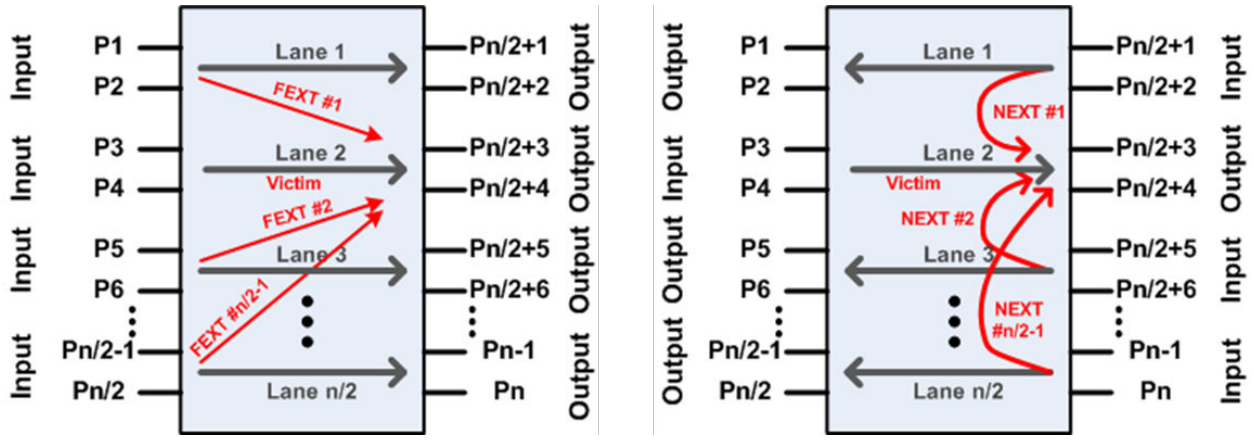
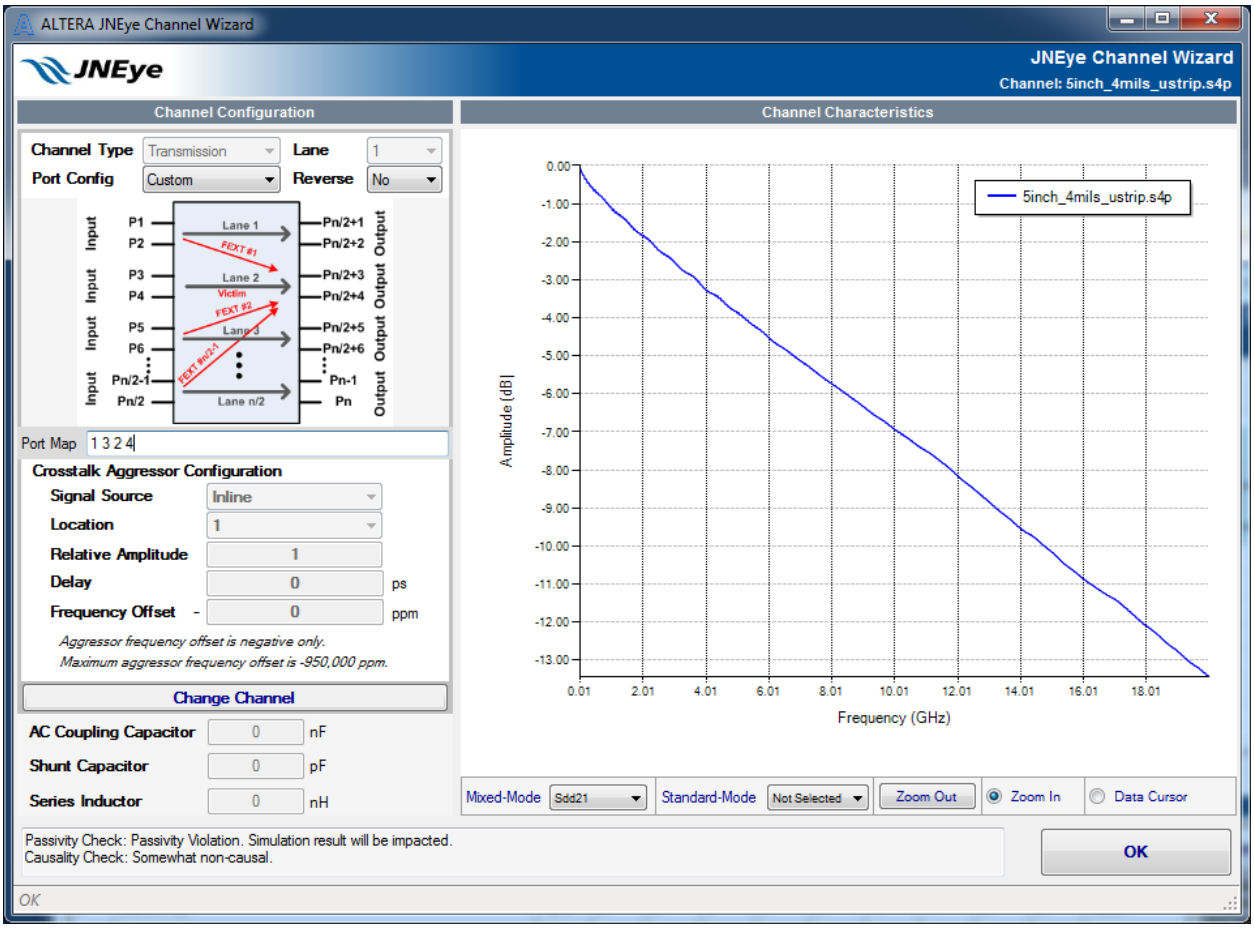


Figure 2-48: S-parameter with Custom Port Configuration



If the S-parameter file is not Type 1, Type 2, or Type 3, you can use the **Custom** option in the Channel Wizard's Port Config pull-down menu, as shown in the following figure. When a Custom port configuration is selected in the Channel Wizard, a text box named **Port Map** appears below the port configuration figure (one of the configurations in the above figure). Enter the port numbers in the sequence [P1, P2, P3, …Pn], where *n* is the number of ports, as illustrated in the figure above that matches the selected S-parameter model. In the figure below, the Port Map sequence 1 3 2 4 corresponds to a 4-port (*n*=4) S-parameter model with port configuration Type 2 where P1=1, P3=Pn/2+1=2, P2=3, and P4=Pn/2+2=4. When a custom port configuration is assigned to an S-parameter model, it is displayed as port configuration Type 4 in the channel table.

Figure 2-49: Custom Port Configuration in Channel Wizard



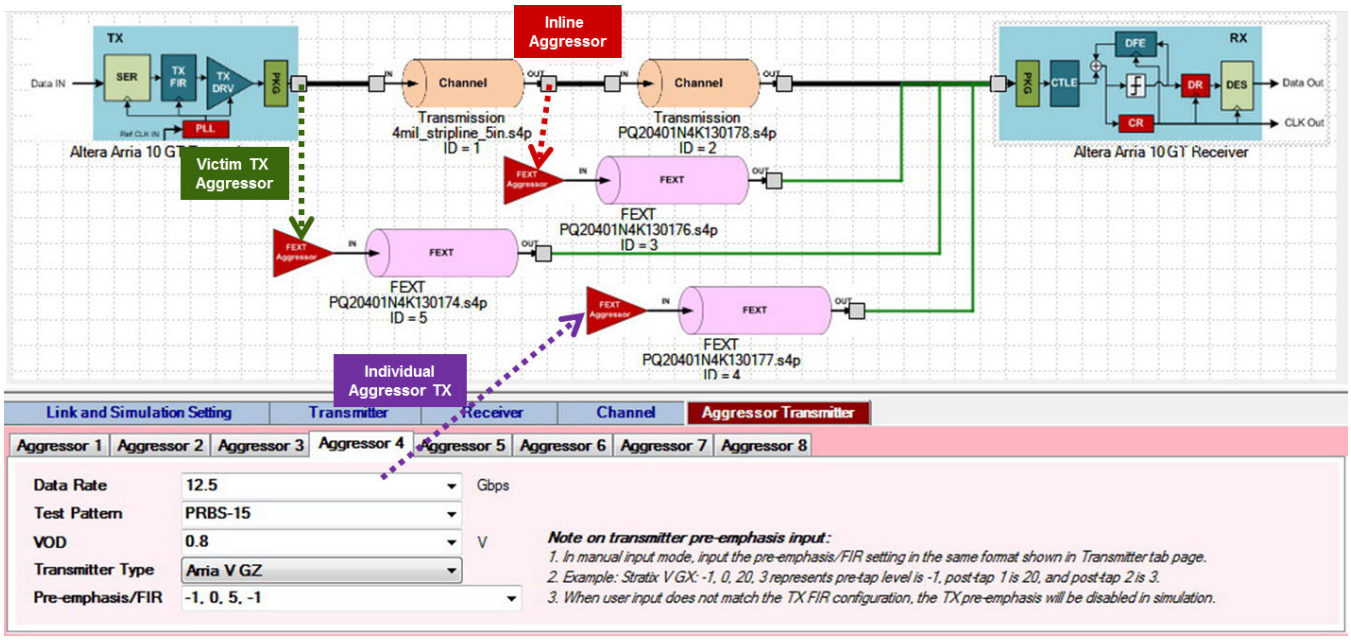
- **Lane**—This field lists the channel lane ID number. For channel lane S-parameters that are 8-port and above, a channel lane must be chosen for link simulations. For example, the above figures show a 12-port 3-lane S-parameter. After loading the channel file, JNEye assigns the center lane as the default simulating channel (or victim channel for crosstalk simulations). Use the **Channel Wizard** to change the lane ID. For 2-port or 4-port S-parameter models, the lane ID is ignored.
- **Rev**—This field indicates whether the channel signal flow direction is to be reversed. This is generally used for the device package model when you want to make sure transmitter and receiver devices are connected to the die side of the package S-parameter model. Refer to the S-parameter comment section for S-parameter signal flow configuration.
- **AC Cap**—This field records AC coupling capacitor value in nF (nano-Farad, 10^{-9} F).
- **Shunt Cap**—This field records shunt capacitance value in pF (pico-Farad, 10^{-12} F).

A crosstalk aggressor has the following parameters:

- **Source**—Each crosstalk aggressor can be of **Inline**, **Transmitter**, or **Aggressor** type.
  - With an **inline** aggressor, the input to the crosstalk channel is the input waveform at the last transmission/victim channel segment.
  - With a **transmitter** aggressor, the aggressor waveform is the same as the victim transmitter with the above aggressor effects, such as frequency offset, delay, and relative amplitude, applied.
  - If the **aggressor** type is "Aggressor X", the aggressor is modeled by the Xth aggressor type as shown in the Aggressor Transmitter tab (refer to the *Crosstalk Aggressor Transmitter Setting* section).

  The following figure shows the three crosstalk aggressor transmitter types. Inline aggressor means the signal feeding into the crosstalk channel comes from the immediate victim channel in parallel with the XTLK channel (as shown in the red dotted arrow line). TX Aggressor means that, regardless of where the XTLK channel is located, this XTLK always uses the VICTIM TX output as its signal source (shown in the green dotted line). The Individual Aggressor TX is similar to the Victim TX Aggressor, but it can be generated separately.

Figure 2-50: Crosstalk Aggressor Types

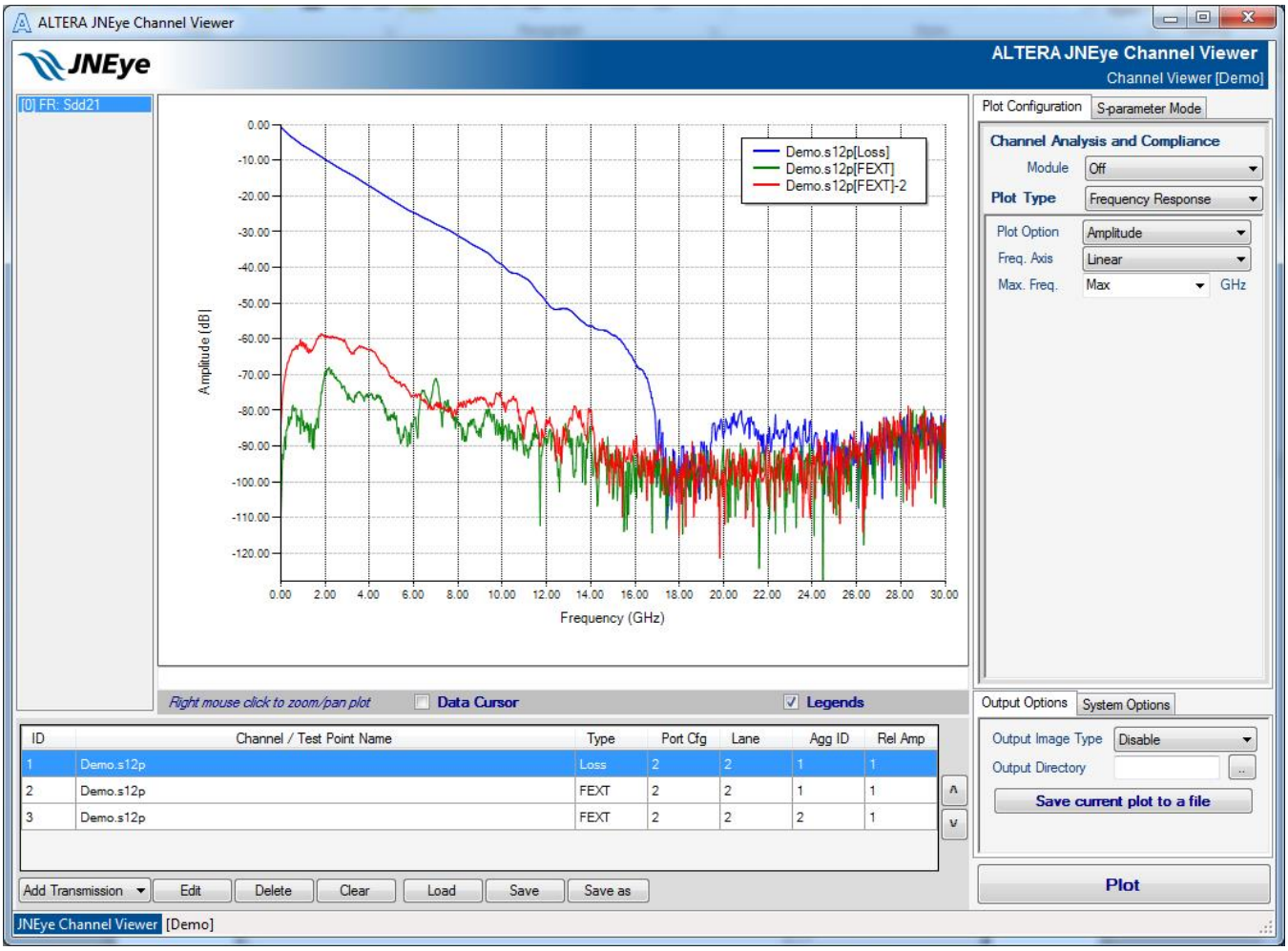


- **Location**—For multiple channel/lane S-parameters simulating crosstalk effects, you must specify the aggressor location. For example, the above figures show four possible crosstalk configurations from a 12-port S-parameter model. Use the **Aggressor Location** menu in the **Channel Wizard** to change the aggressor location. The Aggressor ID field is ignored for a victim channel (Loss type).

  Note: The Aggressor ID index excludes victim lanes. For example, in a 12-port S-parameter, there are three lanes. If the middle lane (Lane ID 2) is a victim lane, the two aggressor channels have Aggressor ID 1 and 2, not 1 and 3.
- **Relative Amplitude**—Each crosstalk aggressor can have different aggressor amplitude relative to its original amplitude. The default value for aggressor is 1.0, which indicates the aggressor has its original amplitude. The Aggressor ID field is ignored for a victim channel (Loss type).
- **Delay**—Each crosstalk aggressor can have individual delay or time offset. The delay is input in picoseconds (ps, 10^{-12} second). Positive values in aggressor delay indicate the aggressor is lagging behind the victim waveform. Negative values indicate the aggressor is ahead of the victim signal waveform. The Aggressor ID field is ignored for a victim channel (Loss type).
- **Frequency Offset**—Each crosstalk aggressor can run on an offset frequency compared to the victim channel's transmitter. The frequency offset is given in negative ppm (parts per million). The maximum frequency is –950,000 ppm.

The Channel Viewer button is a convenient way of observing channel characteristics in the current channel list. Click **Channel Viewer** to transfer the channels to a new Channel Viewer window. You can then observe various parts of channel characteristics in either frequency- or time-domain. Use the JNEye Channel Viewer to view cascaded channel characteristics if multiple channel components are used in the victim signal path. The following figure illustrates the Channel Viewer plot of the channel construct shown in **Figure 2-44**.

Figure 2-51: JNEye Channel Viewer Example



Refer to the *Tutorial: PCI Express 8GT* chapter for step-by-step channel setup instructions.

Automatic S-parameter Configuration Check (ASCC)

JNEye uses a proprietary **Automatic S-parameter Configuration Checker (ASCC)** to help you set and connect the S-parameter in the channel chain. With ASCC, JNEye inspects the S-parameter model and determines the port number and port configuration. ASCC also selects the middle lane as the victim channel (insertion loss channel) and sets the Lane and Aggressor pull-down menus for user configuration. Channel configuration information is saved individually for each channel. Therefore, S-parameters with different port numbers and/or port configurations can be mixed and cascaded in JNEye.

Related Information

- **Tutorial: PCI Express 8GT** on page 3-1
- **Crosstalk Aggressor Transmitter Setting** on page 2-73

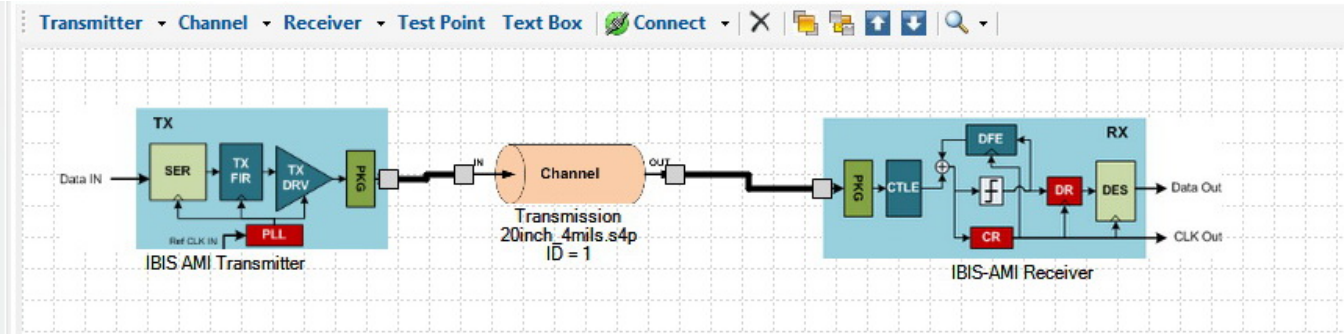
Batch Channel Simulation Configuration

JNEye provides a convenient way to set up batch channel simulations. Batch channel simulation generation can be accomplished when the following conditions are met:

- A complete link is graphically configured. This requires that:
  - The link contains a transmitter, receiver, and at least one transmission channel.
  - In the Link Designer, the connection lines from the transmitter to the receiver are bold black lines.
- The link configuration is complete and ready for simulating with a variety of channels. Link configurations such as data rate, test pattern, BER target, reference clock setting, transmitter and receiver operation mode, and link optimization method are set and ready for simulations.

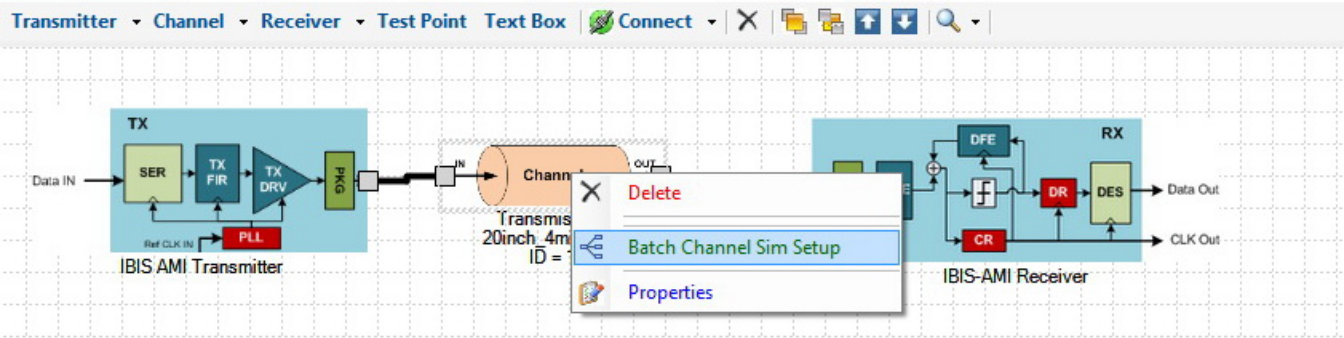
When these conditions are met, perform the following steps to set up a batch simulation. This example creates a batch simulation using the same transmitter, receiver, and other link settings while evaluating a group of channels at the place of the channel **20in_4mils.s4p**, as shown in the following figure.

Figure 2-52: Example Link Configuration for Creating Batch Channel Simulations



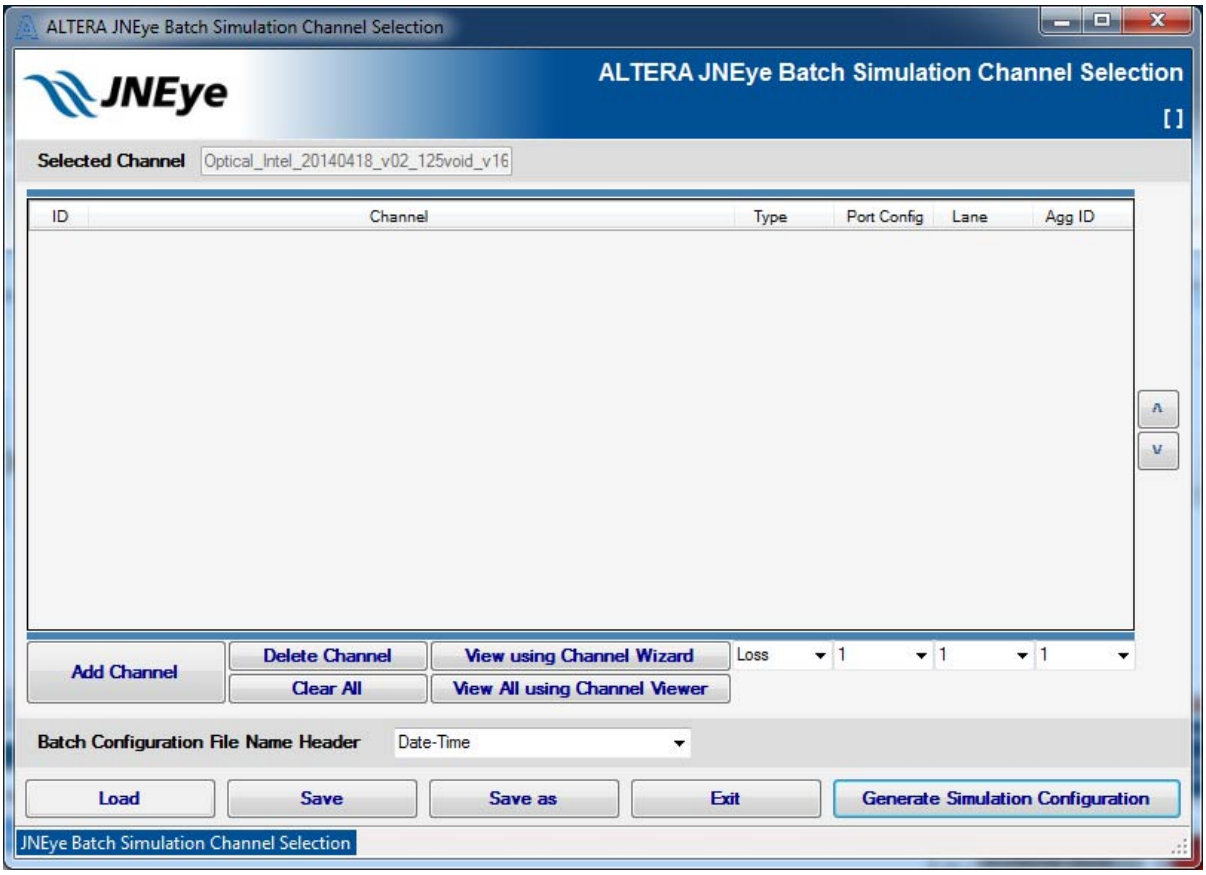
1. Choose a connected channel from the Link Designer work space. Right-click on the channel to bring up a context menu.

Figure 2-53: Batch Channel Simulation Configuration Selection



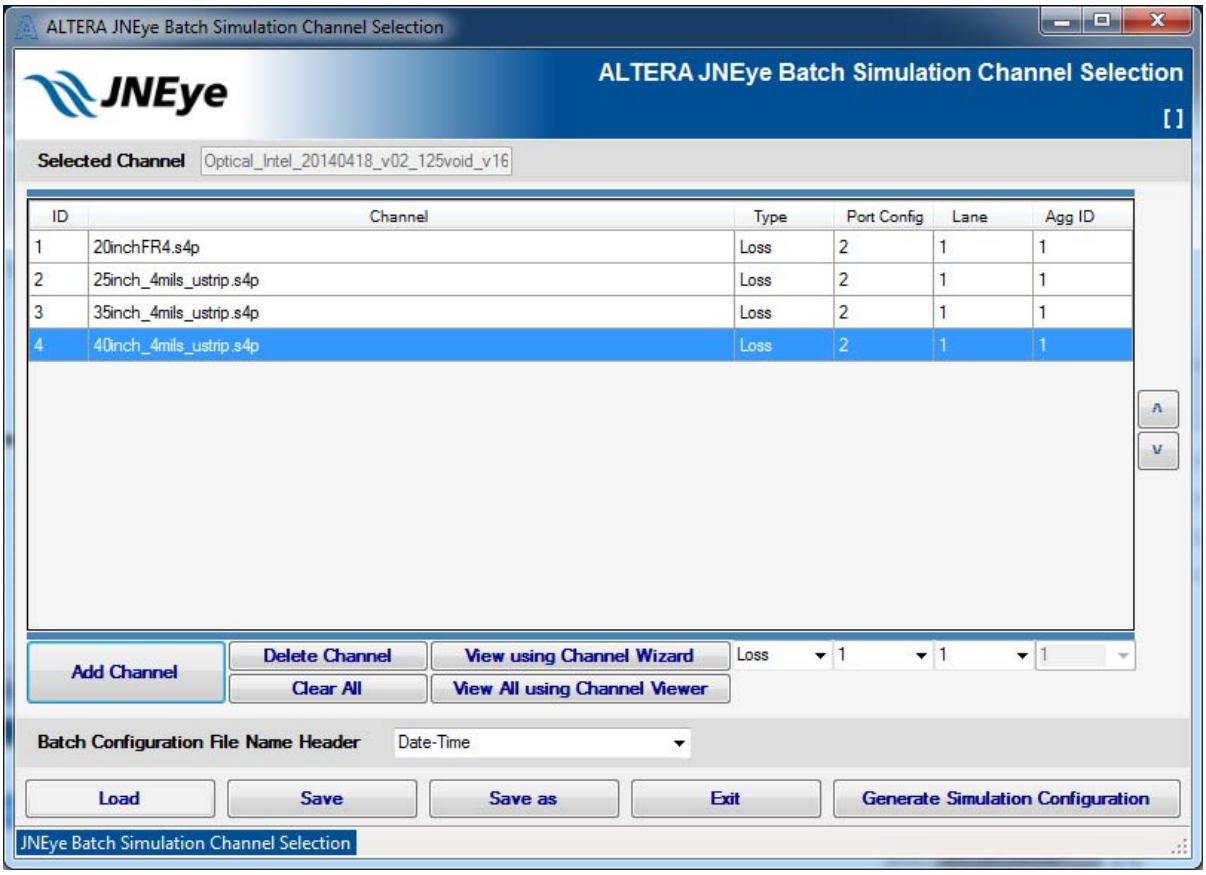
The JNEye Batch Simulation Channel Selection window appears.

Figure 2-54: Batch Simulation Channel Selection Window



2. Click **Add Channel** to select channel files. A file browser helps you select the channel files you want. You can select multiple channels within the file browser. You can also click **Add Channel** repeatedly to add more channels. The added channel is listed in the Channel list box with channel type, port configuration, lane (if the channel is 8-port or more), and aggressor identification (if the channel is a crosstalk channel within a multiple-lane S-parameter).
   - JNEye uses the **Automatic S-parameter Configuration Check (ASCC)** algorithm to automatically detect S-parameter models' port configuration and designate default transmission lane.
   - To observe a channel's characteristics or change a channel's configuration, you can:
     - Select the channel and then click **View using Channel Wizard**. The JNEye Channel Wizard helps you configure the channel.
     - To see all channels' characteristics, click **View All using Channel Viewer** to start the Channel Viewer (refer to the *JNEye Channel Viewer Module* sections for details).
     - Use the pull-down menus or buttons below the channel list boxes to change individual channel configuration.
   - Optionally, you can edit the batch simulation file name header in the pull-down menu or the text box below the channel list boxes. By default, JNEye uses the **Date-Time** string as the file name header. You can also type the desired header name in this box.

Figure 2-55: Example of Batch Channel Selections

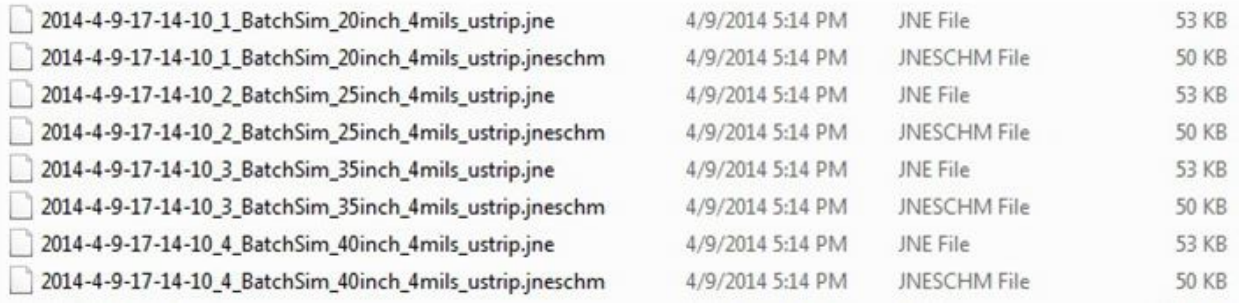


3. When channel selection is complete, click **Generate Simulation Configuration** to generate JNEye simulation configuration files with the selected channels.

   Note: In the current implementation of JNEye, all of the simulation configuration files generated from step 3 will be saved in JNEye installation directory.

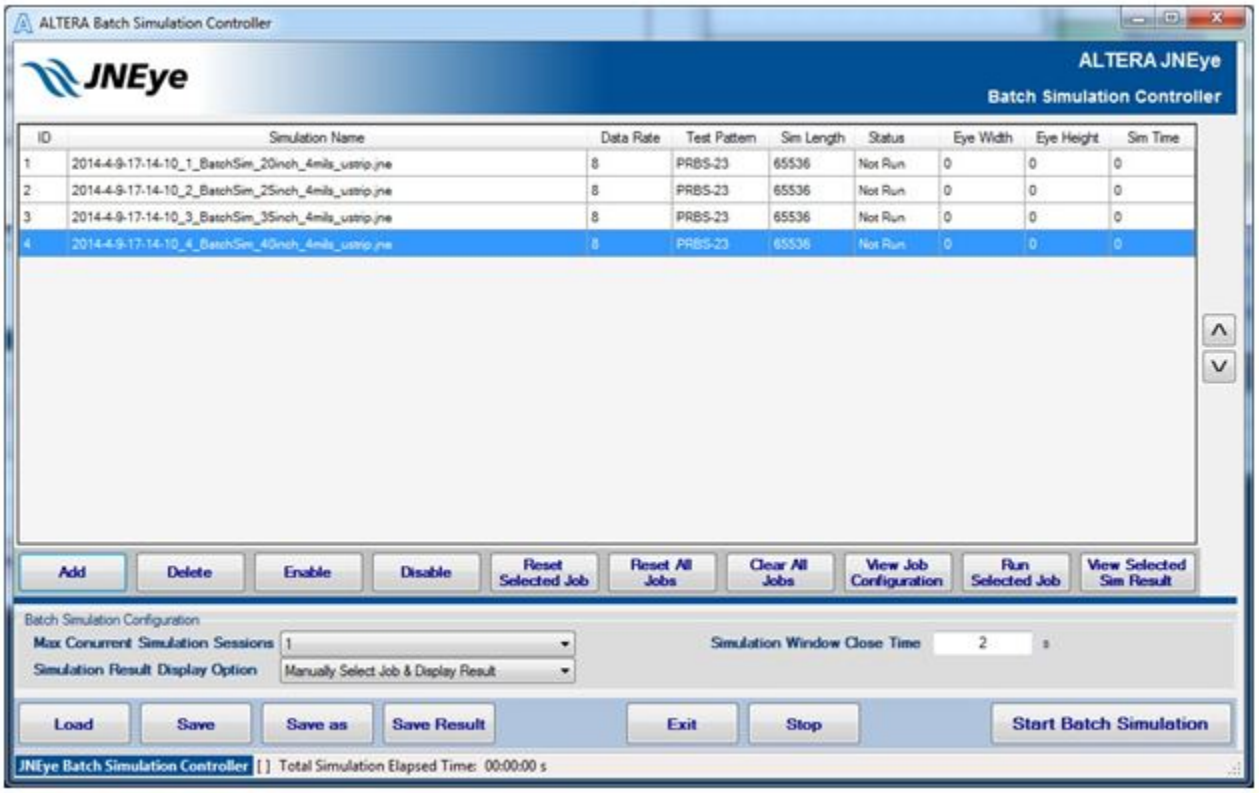
After completing these steps, a series of JNEye simulation configuration files are generated. For example, by using the Date-Time header option, four sets of JNEye simulation configuration files are generated.

Figure 2-56: Batch Generated JNEye Simulation Configuration Files


2014-4-9-17-14-10_1_BatchSim_20inch_4mils_ustrip.jne 4/9/2014 5:14 PM JNE File 53 KB
2014-4-9-17-14-10_1_BatchSim_20inch_4mils_ustrip.jneschm 4/9/2014 5:14 PM JNESCHM File 50 KB
2014-4-9-17-14-10_2_BatchSim_25inch_4mils_ustrip.jne 4/9/2014 5:14 PM JNE File 53 KB
2014-4-9-17-14-10_2_BatchSim_25inch_4mils_ustrip.jneschm 4/9/2014 5:14 PM JNESCHM File 50 KB
2014-4-9-17-14-10_3_BatchSim_35inch_4mils_ustrip.jne 4/9/2014 5:14 PM JNE File 53 KB
2014-4-9-17-14-10_3_BatchSim_35inch_4mils_ustrip.jneschm 4/9/2014 5:14 PM JNESCHM File 50 KB
2014-4-9-17-14-10_4_BatchSim_40inch_4mils_ustrip.jne 4/9/2014 5:14 PM JNE File 53 KB
2014-4-9-17-14-10_4_BatchSim_40inch_4mils_ustrip.jneschm 4/9/2014 5:14 PM JNESCHM File 50 KB

Launch JNEye Batch Simulation Controller to run the generated link simulations (refer to the *JNEye Batch Simulation Controller* section for details). The following figure shows the generated batch channel simulations added in the JNEye Batch Simulation Controller and ready for batch simulations.

Figure 2-57: Added Generated Batch Channel Simulation Configuration in JNEye Batch Simulation Controller



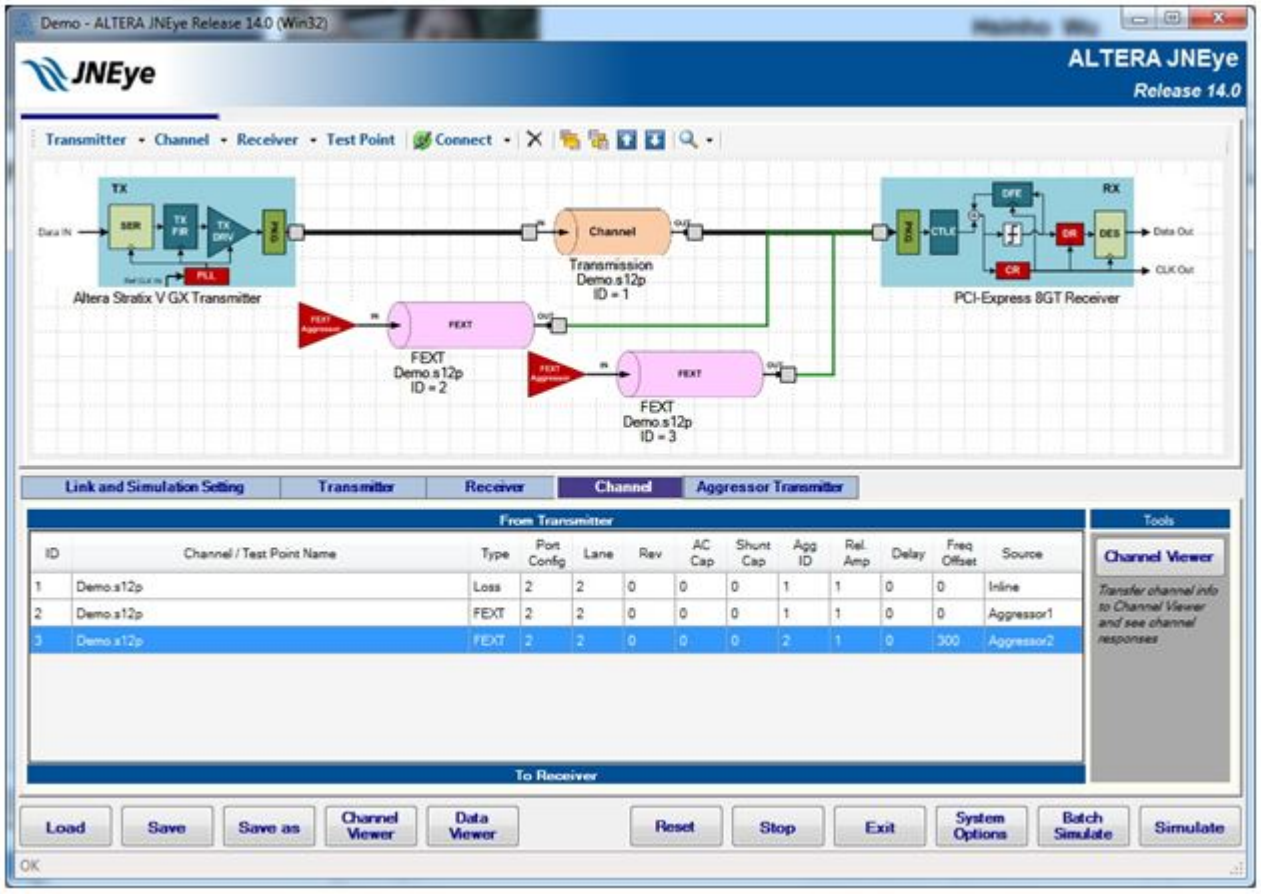
Related Information

- **JNEye Channel Viewer Module** on page 2-98
- **JNEye Batch Simulation Controller** on page 2-129

Crosstalk Aggressor Transmitter Setting

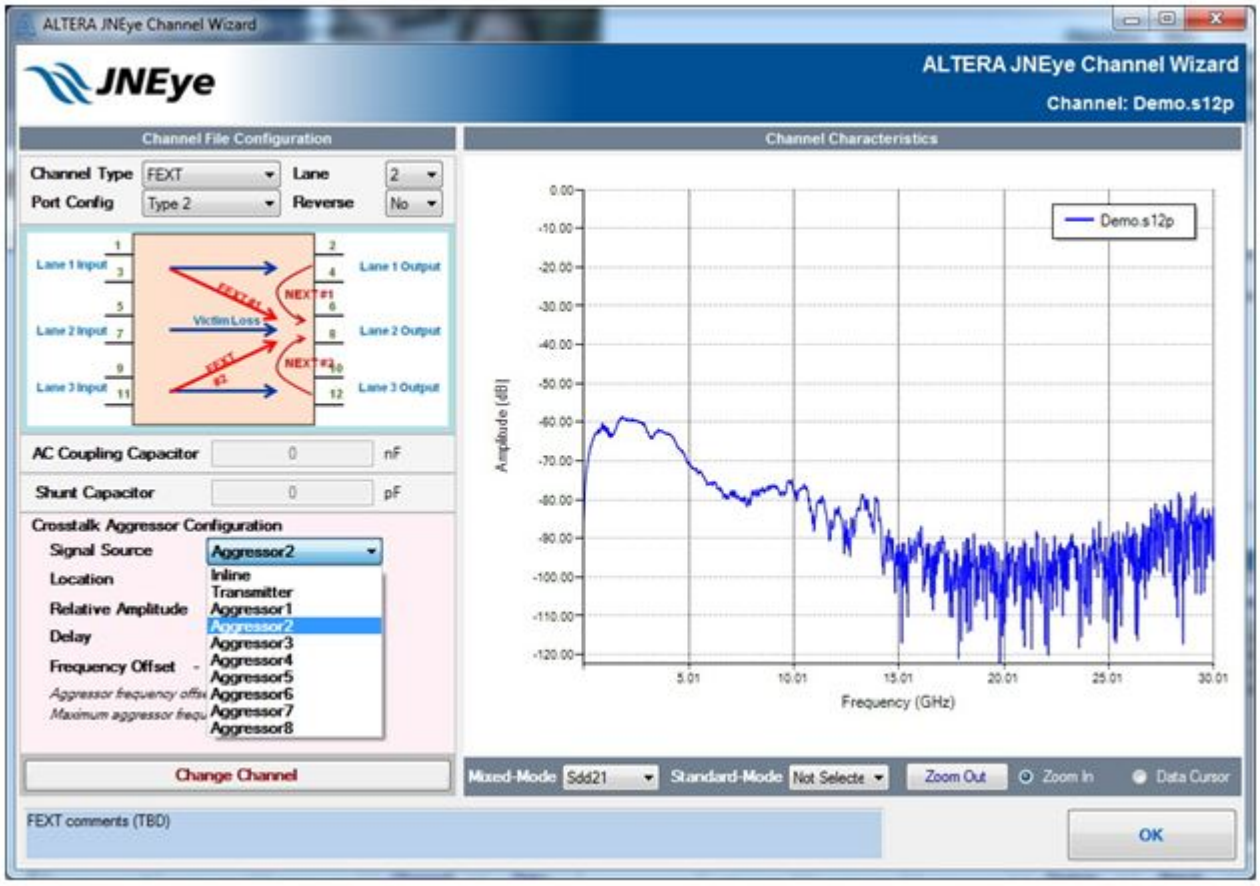
Aggressor transmitter configurations allow you to configure crosstalk aggressors individually with different transmitter types, pre-emphasis settings, amplitudes, data rates, and so forth. The following figure shows a 3-aggressor link with three different aggressor transmitters.

Figure 2-58: Aggressor Transmitter with Three Individual Aggressor Transmitters



Follow the steps described in the previous section to set up a link with crosstalk channels. In the Channel Wizard window, in the Signal Source menu of the Crosstalk Aggressor panel, select the **Inline**, **Transmitter**, or one of the eight available Aggressor types.

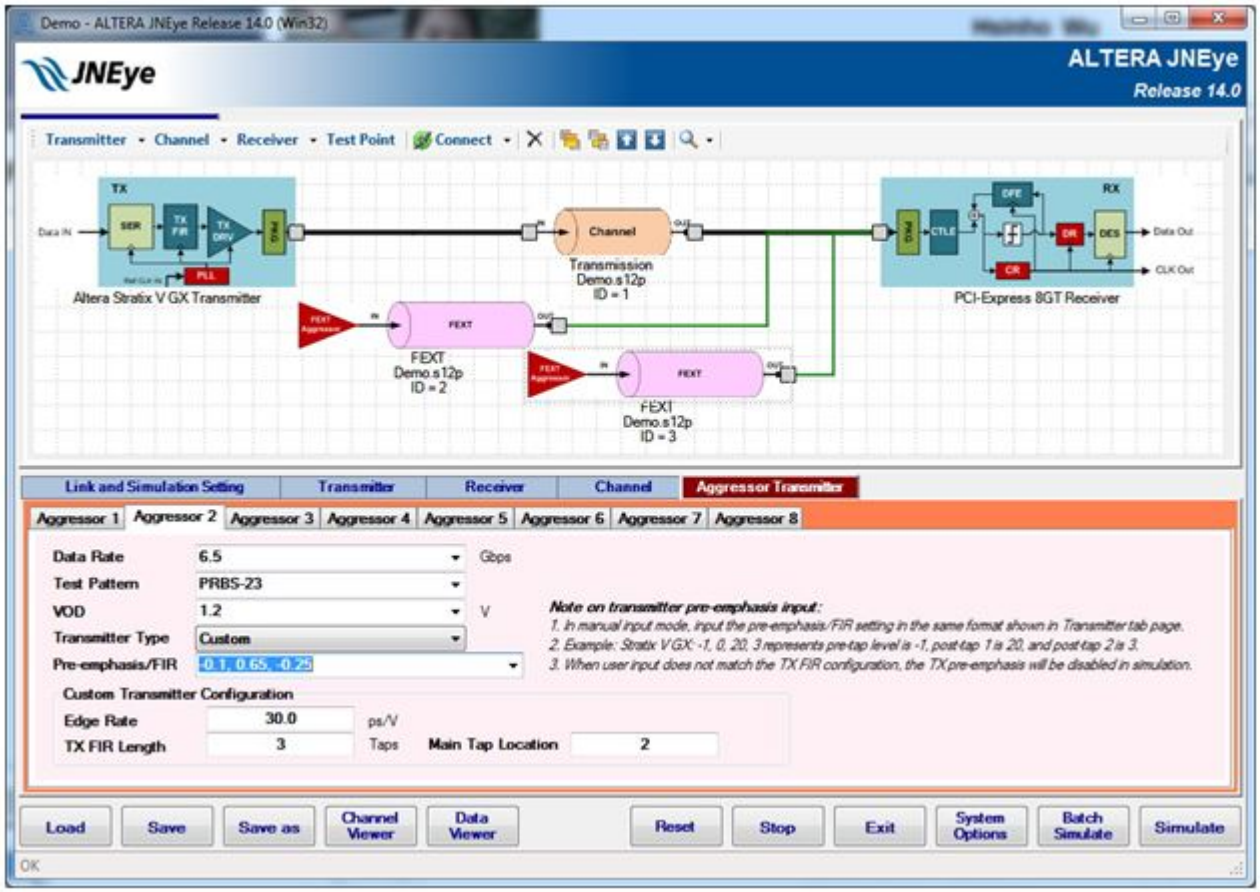
Figure 2-59: Setting Up the Crosstalk Aggressor for a Crosstalk Channel



JNEye supports up to eight individual crosstalk aggressor transmitters. However, a crosstalk aggressor transmitter can be shared among crosstalk channels. By combining the aggressor relative amplitude, frequency offset, and delay setting, JNEye can generate a variety of crosstalk aggressor signal sources.

After completing the configuration in the Channel Wizard, go to the JNEye GUI and select the Aggressor Transmitter tab.

Figure 2-60: Aggressor Transmitter Tab



Within the Aggressor Transmitter tab, there are eight aggressor types associated with the aggressor types in the Channel Wizard's Signal Source menu. Each aggressor can be configured as follows:

- **Data Rate**—Data rate of the selected aggressor transmitter in Gbps.
- **Test Pattern**—Aggressor transmitter's test pattern. JNEye supports the following test patterns:
  - Same as victim TX
  - PRBS-7, PRBS-9, PRBS-11, PRBS-15, PRBS-23, PRBS-31
- **VOD**—Differential output voltage of the aggressor transmitter in volts.
- **Transmitter Type**—Aggressor transmitter can be one of the following transmitter types:
  - Same as victim TX
  - Stratix V GX
  - Arria V GZ
  - Stratix V GT
  - Custom
- **Pre-emphasis / FIR**—Pre-emphasis or FIR setting of the aggressor transmitter. You can set it to be the same as the victim TX or you can type in the setting.

  Note:
  - In manual pre-emphasis/FIR input mode, the pre-emphasis/FIR setting must be in the same format as used in the Transmitter tab. This does not mean that the aggressor transmitter must be the same type as the victim transmitter, but that the pre-emphasis setting format must be in the format as if it is a victim transmitter. For example, if the aggressor transmitter type is Altera Stratix V GX, the pre-emphasis/FIR setting will be in a list of TX-FIR levels such as -1, 0, 20, 3, where -1 is the pre-tap 1 value, 20 is the post-tap 1 value, and 3 is the post-tap 2 value. The main tap can be any value, because JNEye determines the main tap's value based on the values of other FIR taps.
  - If the user input TX pre-emphasis /FIR is invalid for the selected transmitter type, pre-emphasis/FIR will be disabled.

If the transmitter type is Custom, the following parameters are also used:

- **Edge Rate**—JNEye generates a transmitter output waveform with the specified edge rate. Edge rate is in the format of ps/Volt.
- **TX-FIR Length**—Length of TX-FIR for custom aggressor transmitter.
- **Main-Tap Location**—Location of main tap of aggressor transmitter.

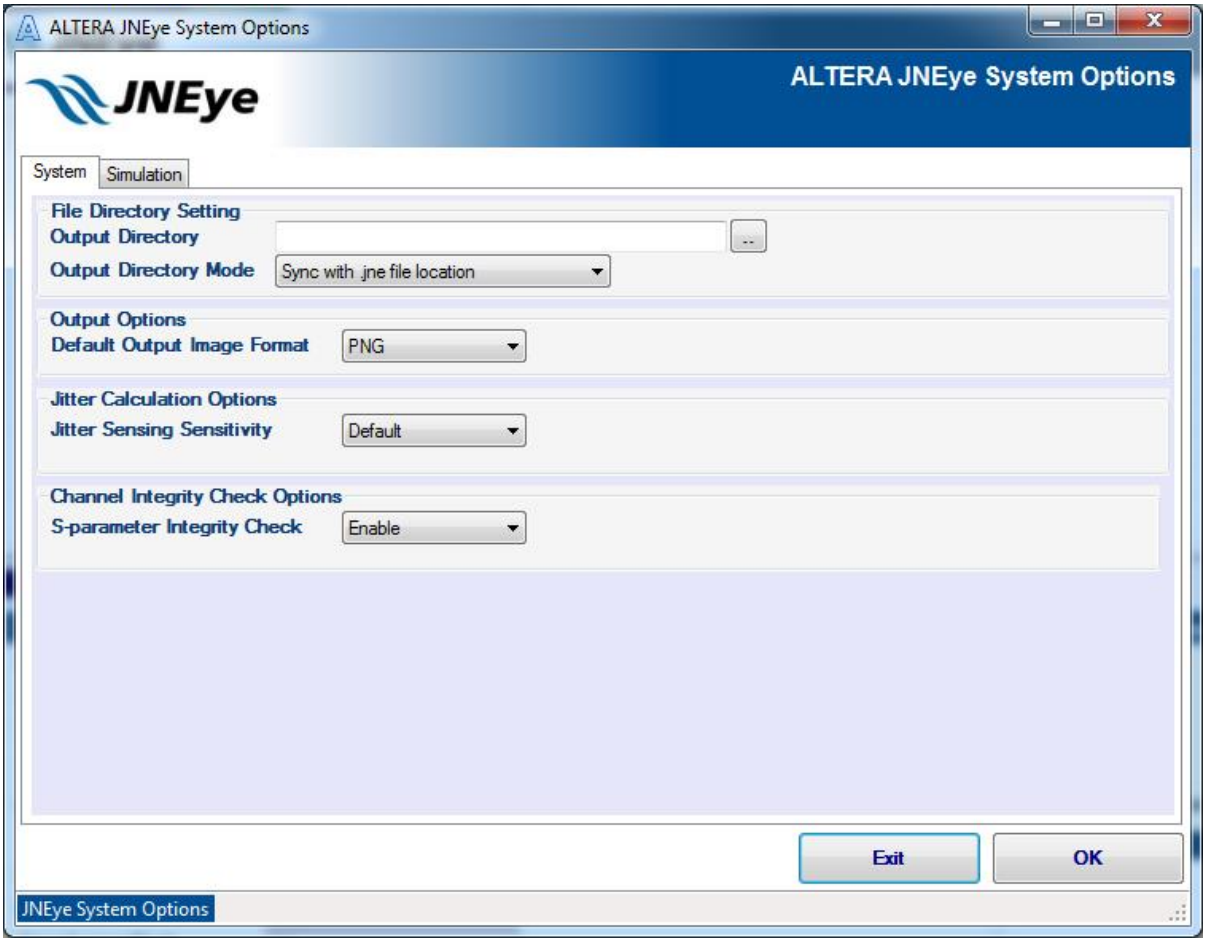
The example shown in **Figure 2-60** indicates an aggressor transmitter, which is a custom transmitter type, running at 6.5 Gbps with the PRBS-23 test pattern and a VOD of 1.2 V. The TX FIR coefficients are [-0.1, 0.65, -0.25] with a TX-FIR length of 3 and the main tap is at 2nd tap. According to the link configuration shown in **Figure 2-58**, this aggressor transmitter is associated with Crosstalk (FEXT) channel ID = 3.

System Options

Use the System Option windows to set the simulation setting.

- **System** tab

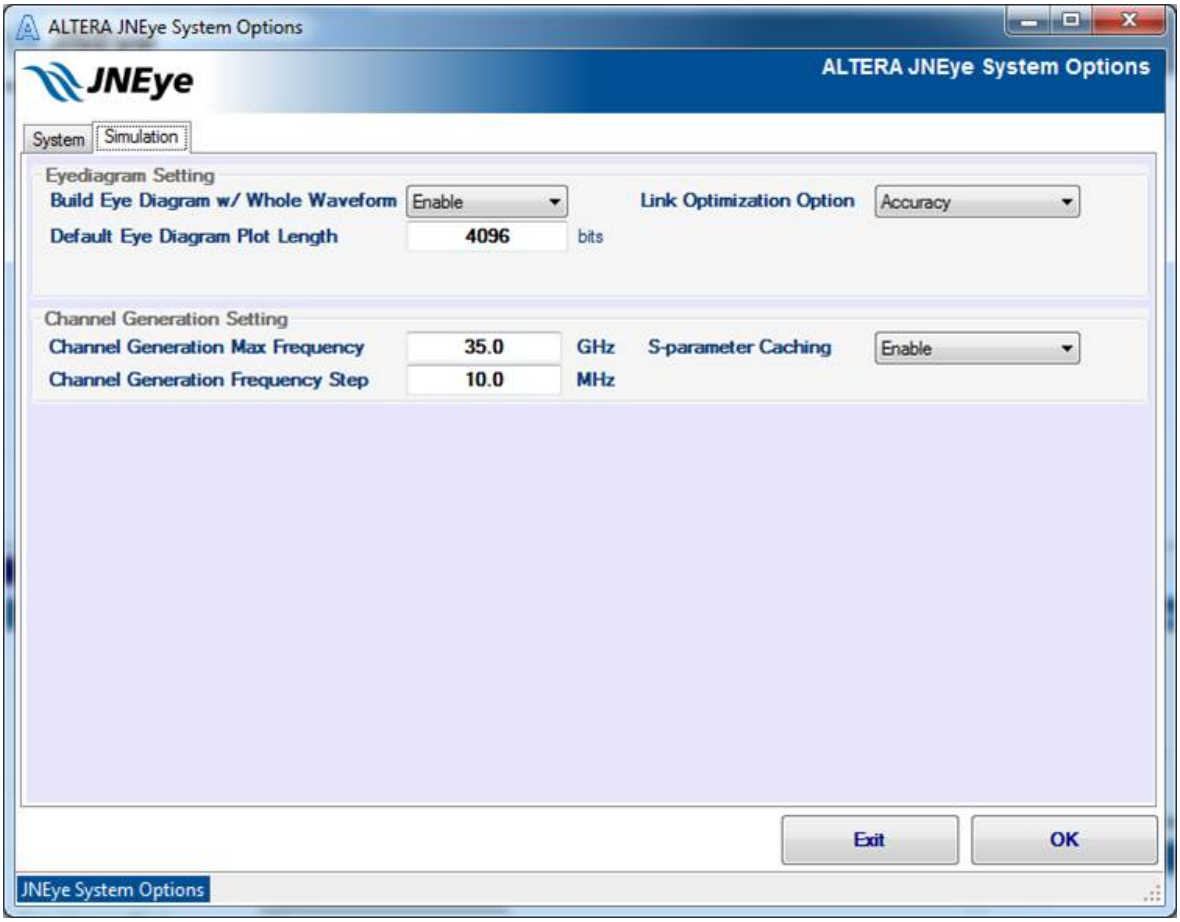
Figure 2-61: JNEye System Options Window: System Tab



- **Output Directory**—Specify an output directory for the simulation results according to the **Output Directory Mode** setting.
- **Output Directory Mode**
  - **Sync with .jne file location**—Automatically sets the output directory to the directory location when **.jne/.jneschm** is created by a user with the **Save** or **Save as** command.
  - **As specified in the Output Directory**—Sets the output directory to the location specified in the **Output Directory** text box.
- **Default Output Image Format**—Set the default output image format to **PNG**, **JPG**, or **GIF**.
- **Jitter Sensing Sensitivity**—Select the sensitivity of jitter detection when JNEye performs jitter analysis (Beta feature in the 15.0 release). The selections are: **Default**, **Ideal**, **Low**, **Medium**, and **High**. The **Default** setting is equivalent to the **Ideal** setting.
- **S-parameter Integrity Check**—Use this entry to enable or disable channel integrity checking in JNEye. The default setting is **Enable**. Choose **Disable** if JNEye has issues in opening or accessing an S-parameter model.

- **Simulation** tab

Figure 2-62: System Options Window: Simulation Tab



- **Default Eye Diagram Plot Length**—This parameter controls the waveform length used to construct the eye diagram when the **Build Eye Diagram w/ Whole Waveform** option is disabled. You can increase the length as long as the length is less than the simulation length. The default value is 4096 bits.
- **Build Eye Diagram w/ Whole Waveform**—If **Enable** is selected, JNEye uses the whole simulated waveform to build the eye diagrams. If the simulation length is large, this will take more time. The default setting is **Enable**.
- **Link Optimization Option**—The choices are **Accuracy** or **Speed**. The default is **Accuracy**. By selecting **Speed**, the link optimization process runs faster at the cost of possibly less optimal solutions.
- **Channel Generation Max Frequency**—Sets the default maximum frequency of the channel models generated in JNEye. The default value is 35 GHz.
- **Channel Generation Frequency Step**—Sets the default frequency step of the channel models generated in JNEye. The default value is 10 MHz.
- **S-parameter Caching**—If **Enable** is selected, the last read S-parameter file is cached in memory for faster access and processing. Doing this greatly improves GUI performance when reading a multiple-lane S-parameter file with large file size. You can disable this feature.

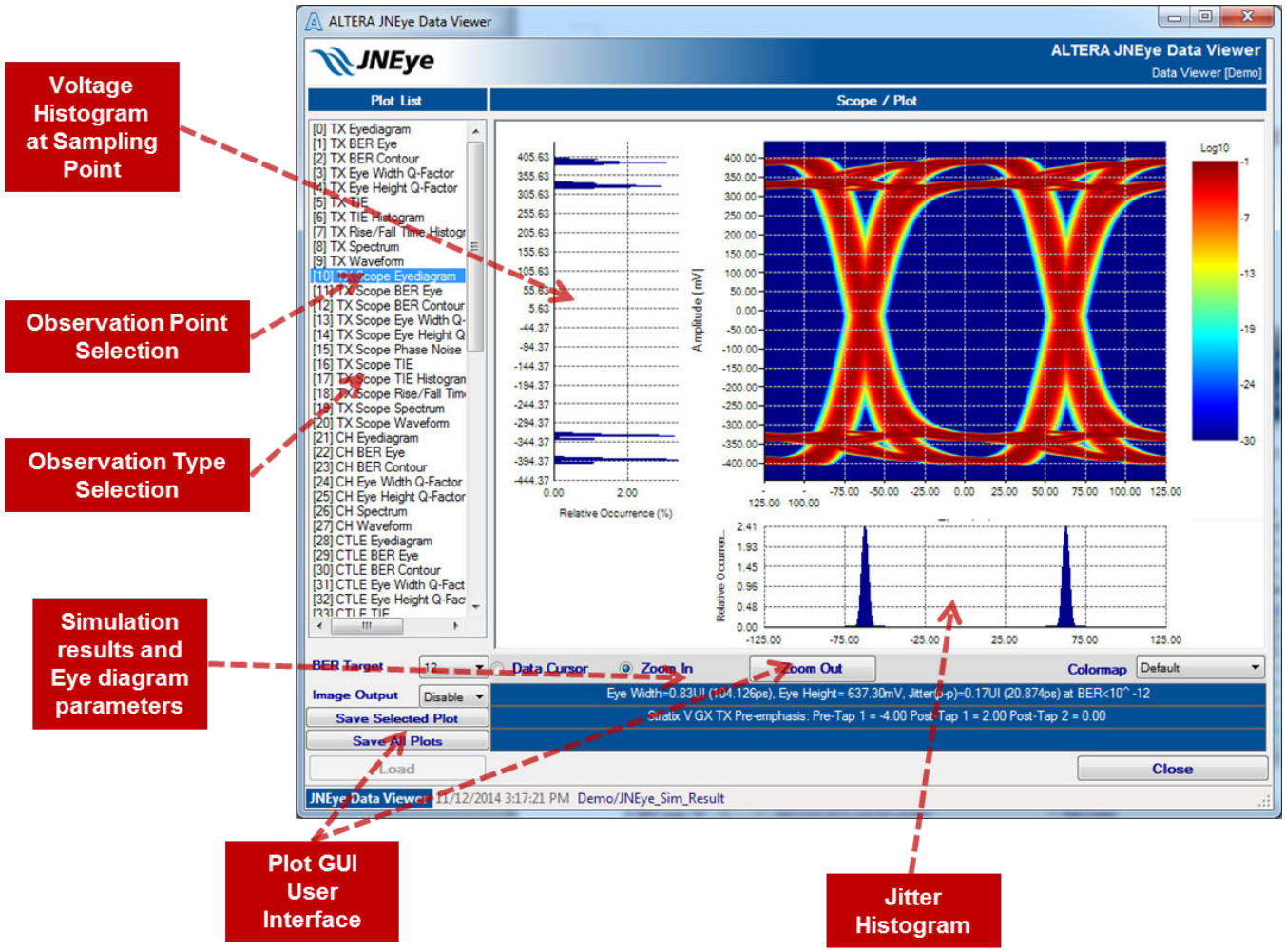
JNEye Data Viewer Module

The JNEye Data Viewer displays simulation and analysis results. The Data Viewer can be started in the following ways:

- Automatically start after the completion of a simulation
- Click **Data View** in JNEye's main GUI
- Double-click **JNEye_Data_Viewer.exe**

JNEye uses the Data Viewer to show various types of simulation and analysis results. It can show multiple plots. Use the list box in the left panel to select the plots.

Figure 2-63: JNEye Data Viewer User Interface



The following GUI capabilities are provided in the Data Viewer:

- **Zoom control**
  - **In an eye diagram plot**—Click **Zoom In** or click and drag a rectangle box to show the details of a plot. Click **Zoom Out** to restore the plot scale.
  - **Others**—Right-click to bring up a menu with **Zoom Out**, **Select**, **Zoom**, **Pan**, and waveform commands.
- **Data Cursor**—Select **Data Cursor** to show the data cursor boxes. You can select and drag a data cursor box with the data values shown in the box. The data values are colored according to the data lines.

  Note: The **Data Cursor** button may not be present in certain types of plots such as waveform plots. If you move the cursor over a data point, a pop-up window shows the data value.

Figure 2-64: Data Cursor Example

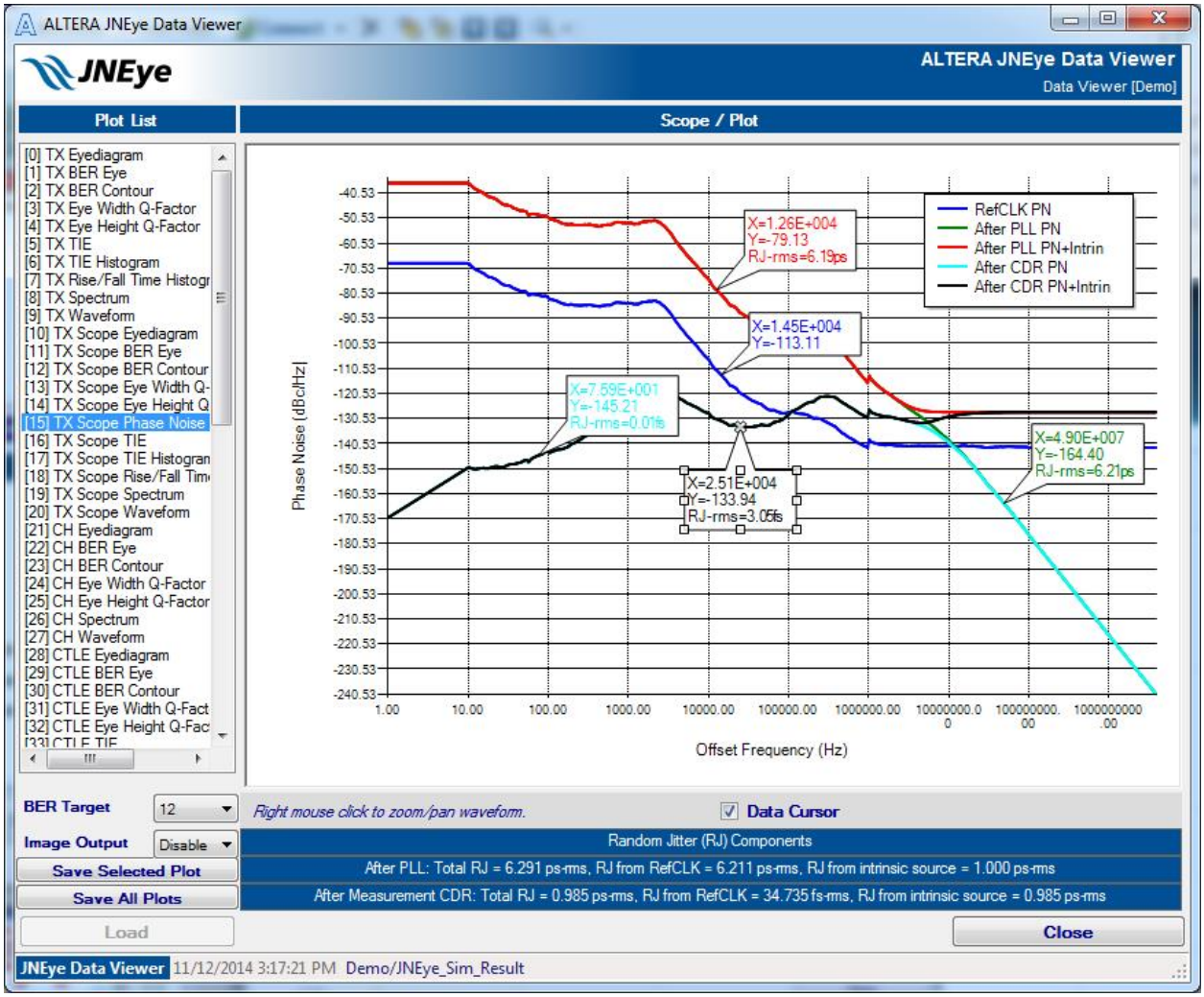
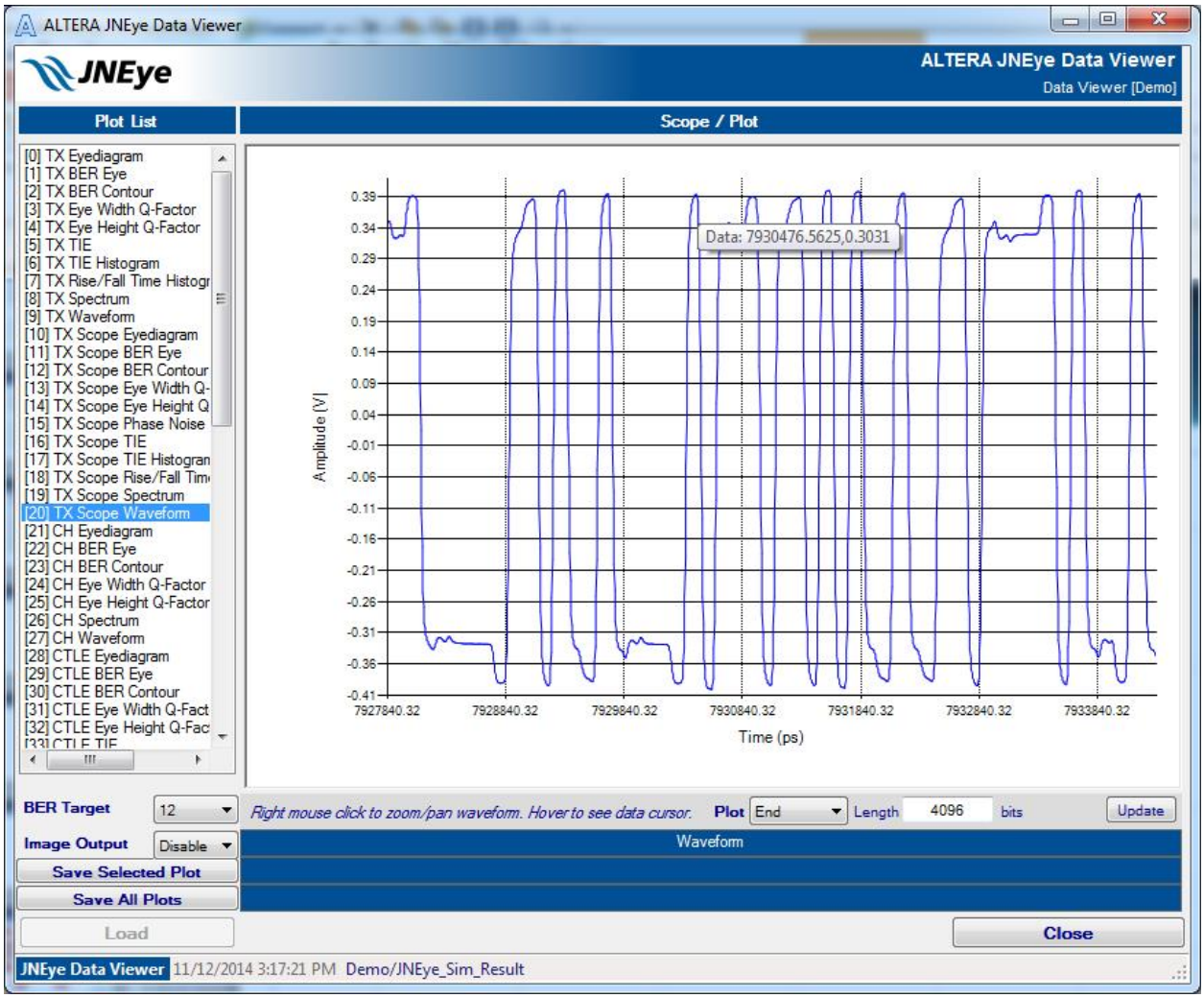


Figure 2-65: Data Cursor Example for Waveform Plot



- **Legends**—Plot legends are shown when plots are generated. Use the **Page-Up**, **Page-Down**, **Home**, and **End** keys on the keyboard to move the legend box. Turn the **Legends** check box on or off to show or hide the legend box.

Within the Data Viewer, you can modify the link's BER target using the BER Target menu. The JNEye Data Viewer recalculates the jitter and the eye-opening height and width dynamically, because the JNEye Simulation Engine has pre-calculated the results at different BER targets in the simulation range.

Use the **Colormap** menu to change the color map of eye diagrams within the Data Viewer. JNEye provides eight different color maps that you can choose from, depending on your analysis purpose and visual preferences. The color maps can be divided into two groups:

- **Logarithmic Color Scale**—Default, Blue, Heat, and Bone
- **Linear Color Scale**—Default Linear, Blue Linear, Heat Linear, and Bone Linear

The logarithmic color scale provides good visual performance in displaying low probability data points such as the low BER portion of an eye diagram. The linear color scale is more suitable for showing minor differences in close-range data values. The Blue/Blue Default Linear is good for showing deterministic

simulation results when no jitter or noise is present. JNEye automatically chooses the most suitable color map based on the type or configuration of a simulation. The default color map is either **Default** or **Blue**.

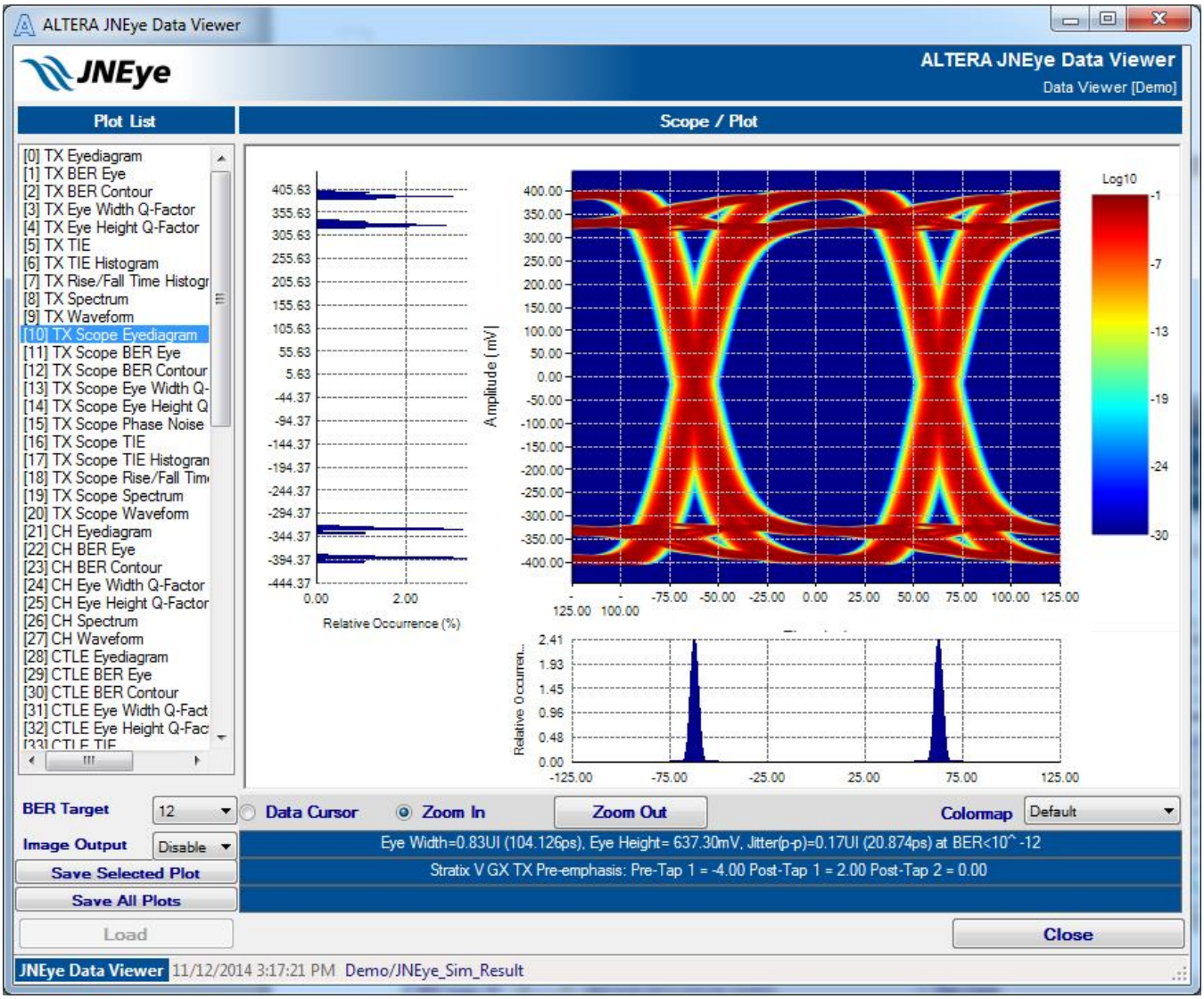
- The **Image Output** menu allows you to generate output images in **.png**, **.jpg**, or **.gif** format. This is useful when you want to generate images after simulation is done previously. (Refer to **Figure 2-77**.)
- When **Save Selected Plot** is clicked, a file browser helps you select the image file to be saved. An image file of the currently selected plot is saved in the format specified in the **Image Output**.
- When **Save All Plots** is clicked, a folder browser helps you select the folder location where all image files will be saved. Image files of all plots are saved in the format specified in the **Image Output**.

The JNEye Data Viewer Module shows the following types of simulation results:

Probability Density Function (PDF) Eye Diagram

This scope shows the PDF eye diagram (with probability color map), horizontal histogram at slicer voltage level (fixed at 0 V in the JNEye), vertical histogram at Ideal Clock or CDR sampling phase, and eye diagram opening width and height information. Device settings such as transmitter pre-emphasis/FIR setting and receiver equalization settings are shown in the text display area below the plots.

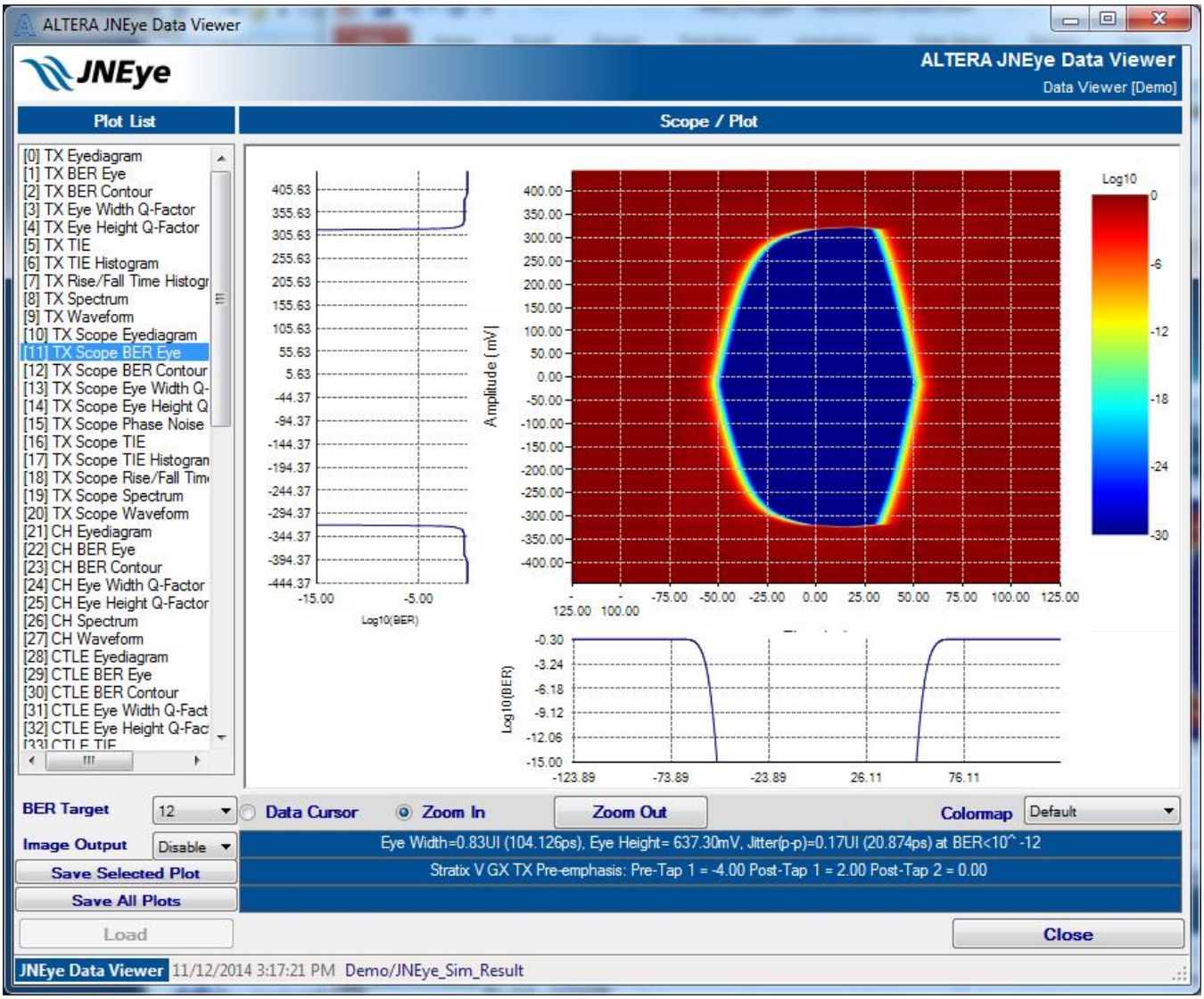
Figure 2-66: JNEye Data Viewer PDF Eye Diagram and Plots



Cumulative Distribution Function (CDF) Eye Diagram

This scope shows the CDF eye diagram (with probability color map), horizontal BER bathtub curve (fixed at 0 V in JNEye), vertical BER bathtub curve (at ideal clock or CDR sampling phase), and eye diagram opening width and height. The eye diagram compliance mask is plotted when it is enabled and applicable.

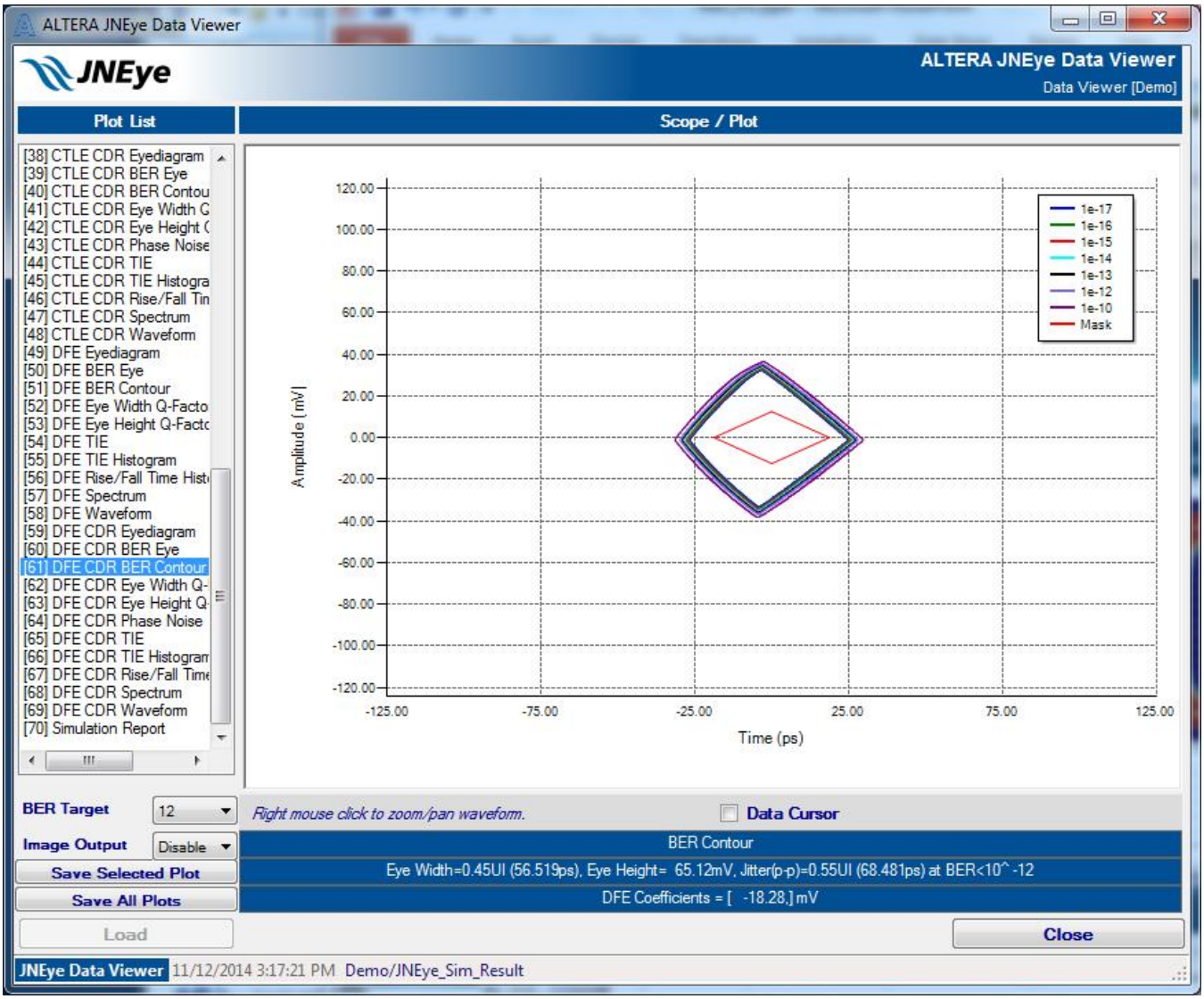
Figure 2-67: JNEye Scope CDF and Plots



BER Contour

The Data Viewer shows the BER contour and eye diagram opening width and height. The eye diagram compliance mask is plotted when it is enabled and applicable.

Figure 2-68: JNEye Scope BER Contour and Plots



Q-Factor Curve

A different view of the BER bathtub curve using Q-factor.

Figure 2-69: JNEye Data Viewer Q-Factor Plot (Time Axis)

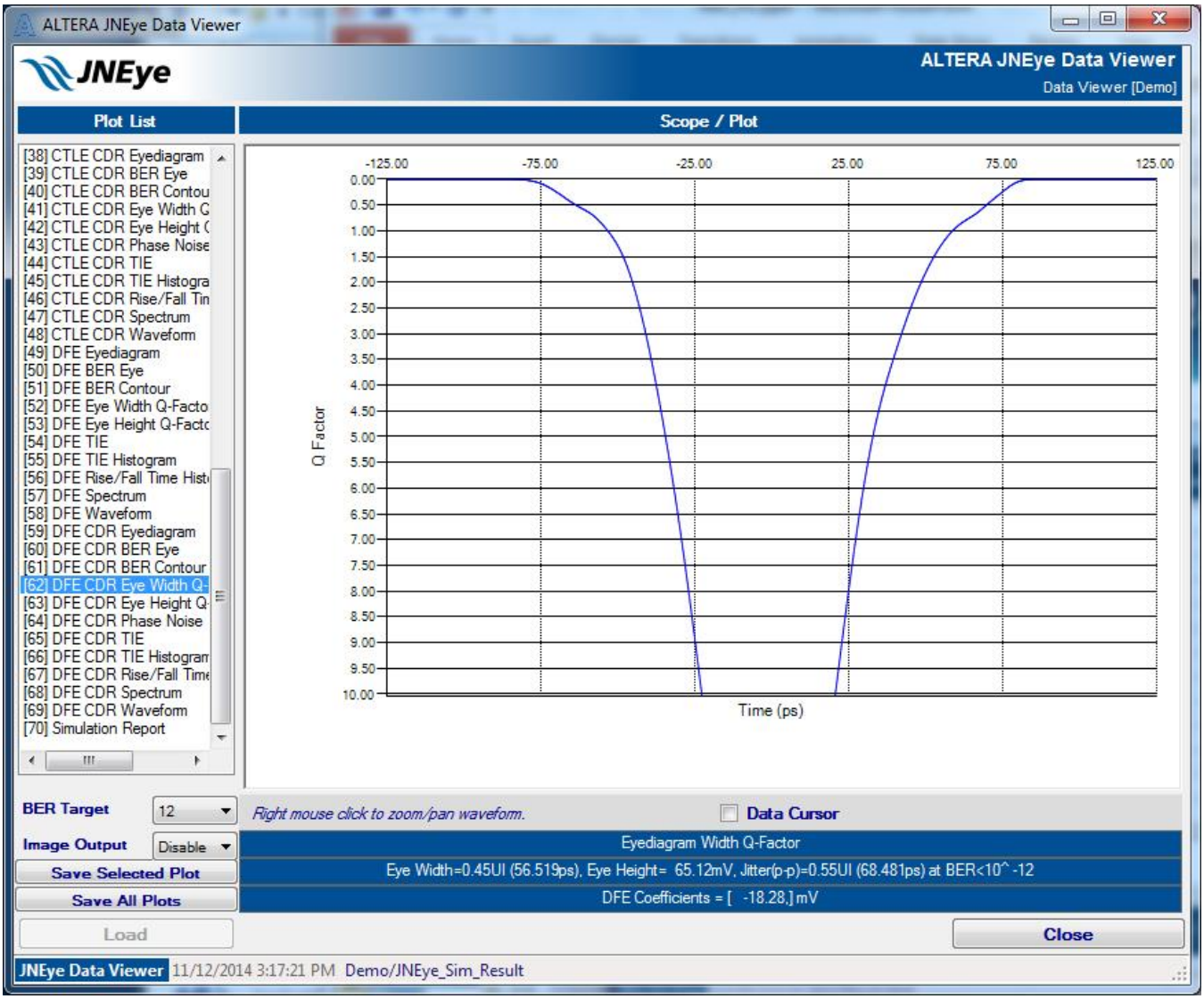
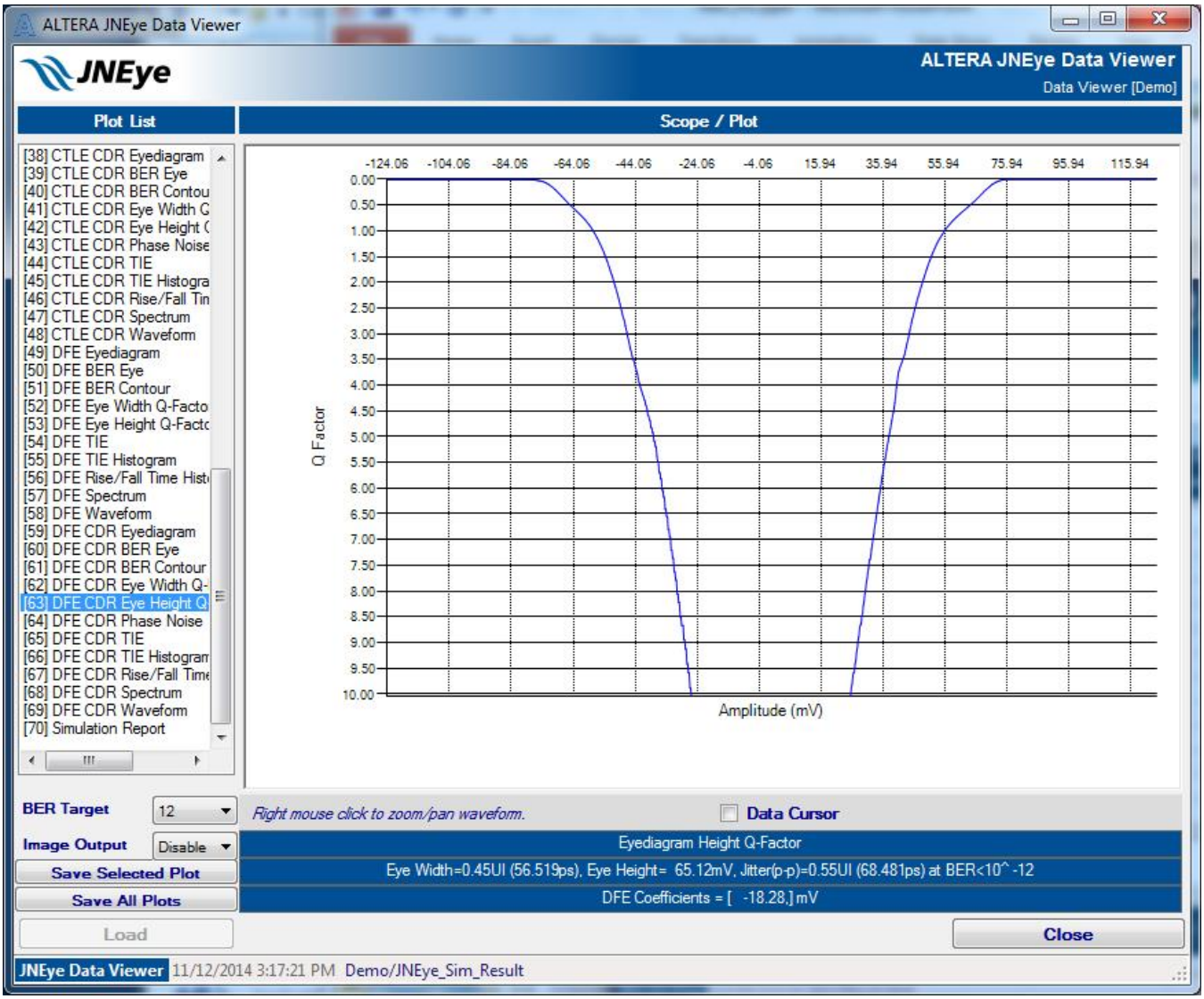


Figure 2-70: JNEye Data Viewer Q-Factor Plot (Amplitude Axis)


ALTERA JNEye Data Viewer
JNEye
ALTERA JNEye Data Viewer
Data Viewer [Demo]
Plot List
Scope / Plot
[38] CTLE CDR Eyediagram
[39] CTLE CDR BER Eye
[40] CTLE CDR BER Contou
[41] CTLE CDR Eye Width C
[42] CTLE CDR Eye Height C
[43] CTLE CDR Phase Noise
[44] CTLE CDR TIE
[45] CTLE CDR TIE Histogra
[46] CTLE CDR Rise/Fall Tin
[47] CTLE CDR Spectrum
[48] CTLE CDR Waveform
[49] DFE Eyediagram
[50] DFE BER Eye
[51] DFE BER Contour
[52] DFE Eye Width Q-Facto
[53] DFE Eye Height Q-Factc
[54] DFE TIE
[55] DFE TIE Histogram
[56] DFE Rise/Fall Time Hist
[57] DFE Spectrum
[58] DFE Waveform
[59] DFE CDR Eyediagram
[60] DFE CDR BER Eye
[61] DFE CDR BER Contour
[62] DFE CDR Eye Width Q-
[63] DFE CDR Eye Height Q
[64] DFE CDR Phase Noise
[65] DFE CDR TIE
[66] DFE CDR TIE Histogram
[67] DFE CDR Rise/Fall Time
[68] DFE CDR Spectrum
[69] DFE CDR Waveform
[70] Simulation Report
-124.06 -104.06 -84.06 -64.06 -44.06 -24.06 -4.06 15.94 35.94 55.94 75.94 95.94 115.94
0.00 0.50 1.00 1.50 2.00 2.50 3.00 3.50 4.00 4.50 5.00 5.50 6.00 6.50 7.00 7.50 8.00 8.50 9.00 9.50 10.00
Q Factor
Amplitude (mV)
BER Target
12
Right mouse click to zoom/pan waveform.
Data Cursor
Image Output
Disable
Eyediagram Height Q-Factor
Save Selected Plot
Eye Width=0.45UI (56.519ps), Eye Height= 65.12mV, Jitter(p-p)=0.55UI (68.481ps) at BER<10^-12
Save All Plots
DFE Coefficients = [-18.28,] mV
Load
Close
JNEye Data Viewer 11/12/2014 3:17:21 PM Demo/JNEye_Sim_Result

Transmitter Reference Clock Phase Noise Analysis and Plots

JNEye plots the phase noise power spectrum through the link. The transmitter reference clock's phase noise travels through the transmitter PLL, emulated scope, channel, and the RX CDR. In this process, phase noise is shaped by the TX PLL, scope (pass through only), and RX CDR. At the same time, the transmitter and receiver also generate their own intrinsic jitter which is mixed with the jitter caused by the shaped phase noise. The JNEye simulation engine processes and records the phase noise characteristics transition and the amount of random jitter the device contributed internally.

Figure 2-71: Transmitter Reference Phase Noise Analysis (At Transmitter Output)

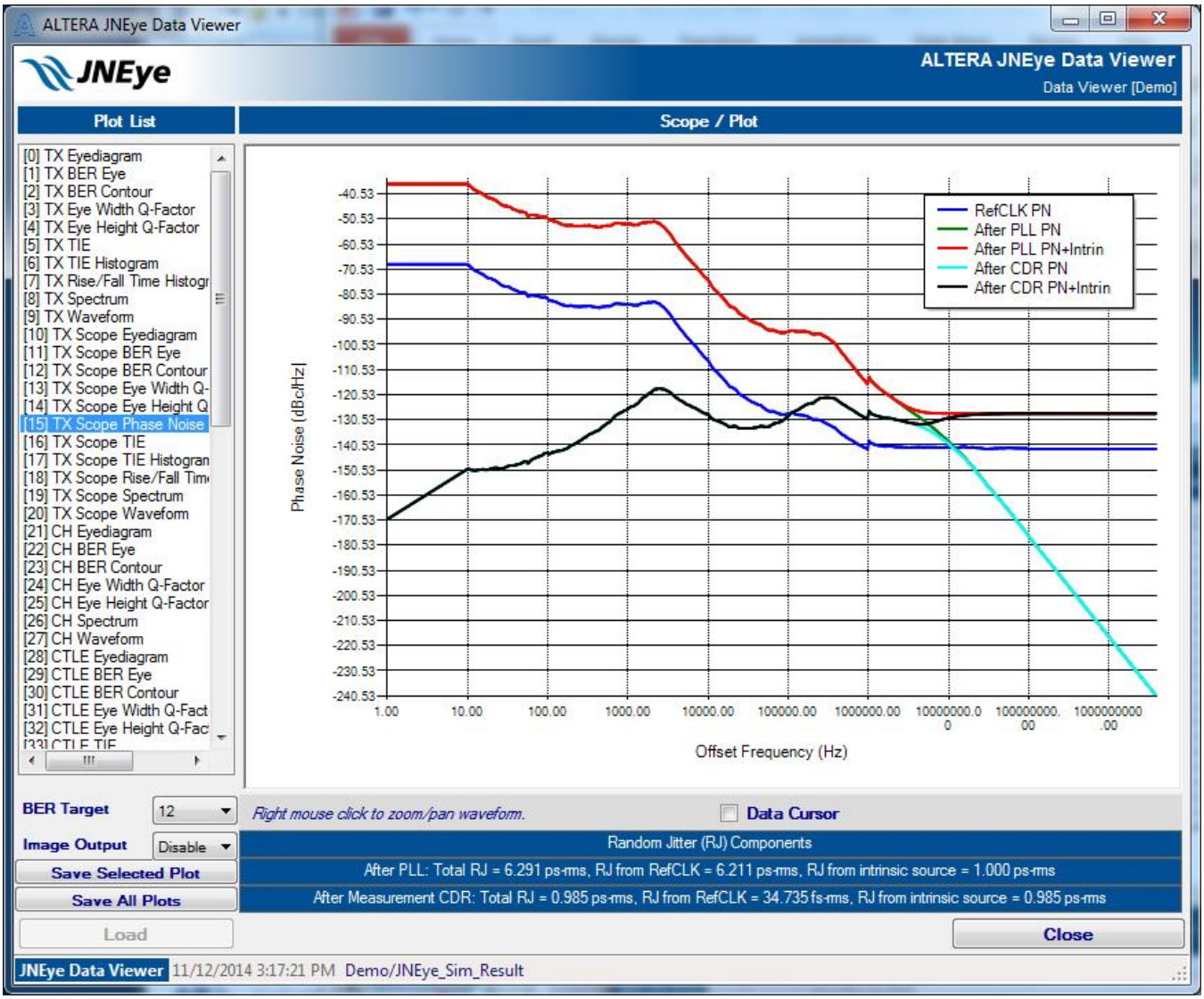
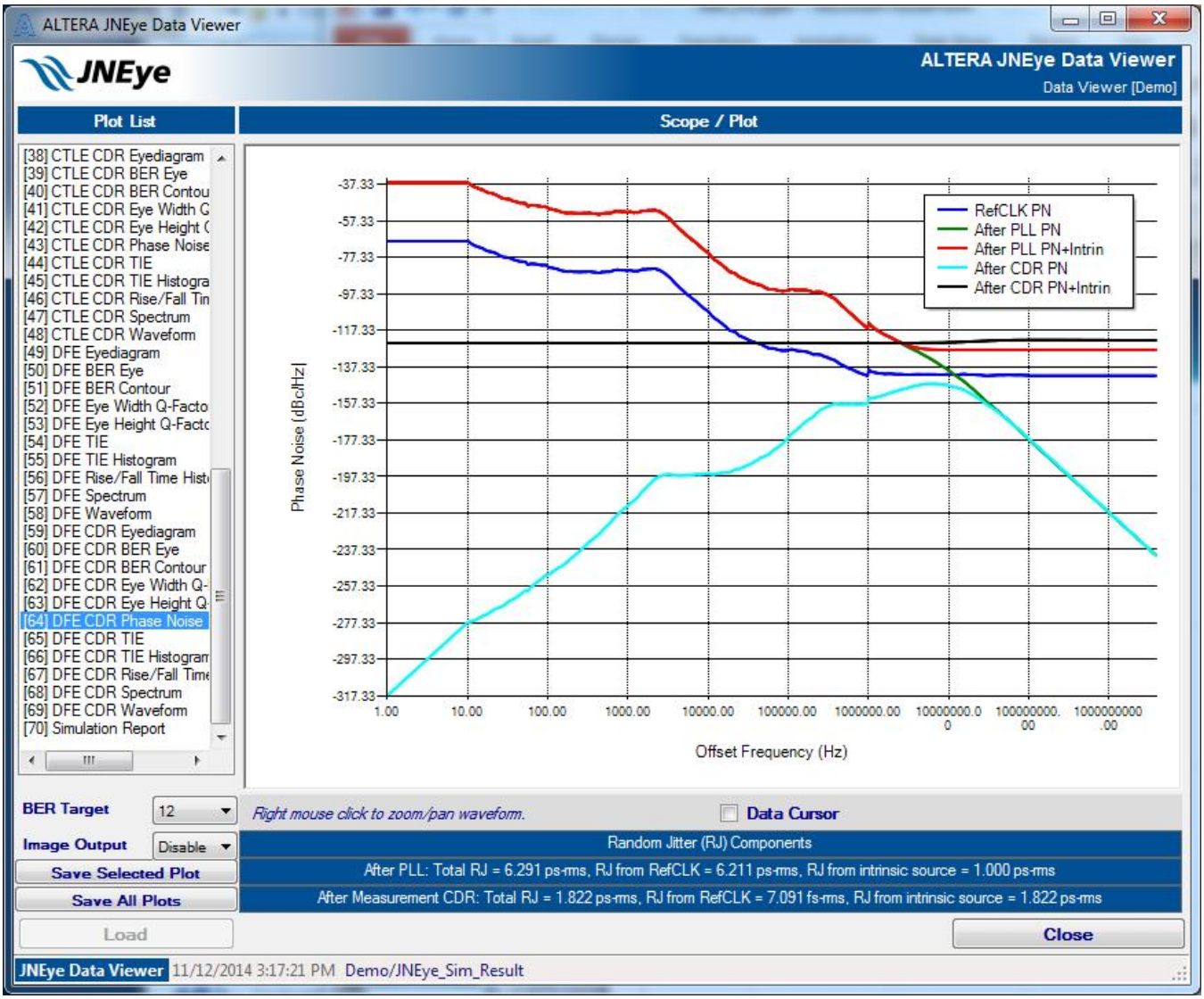


Figure 2-72: Transmitter Reference Phase Noise Analysis (At Receiver Output)



TX pre-emphasis, de-emphasis, or FIR coefficients are displayed with the transmitter output.

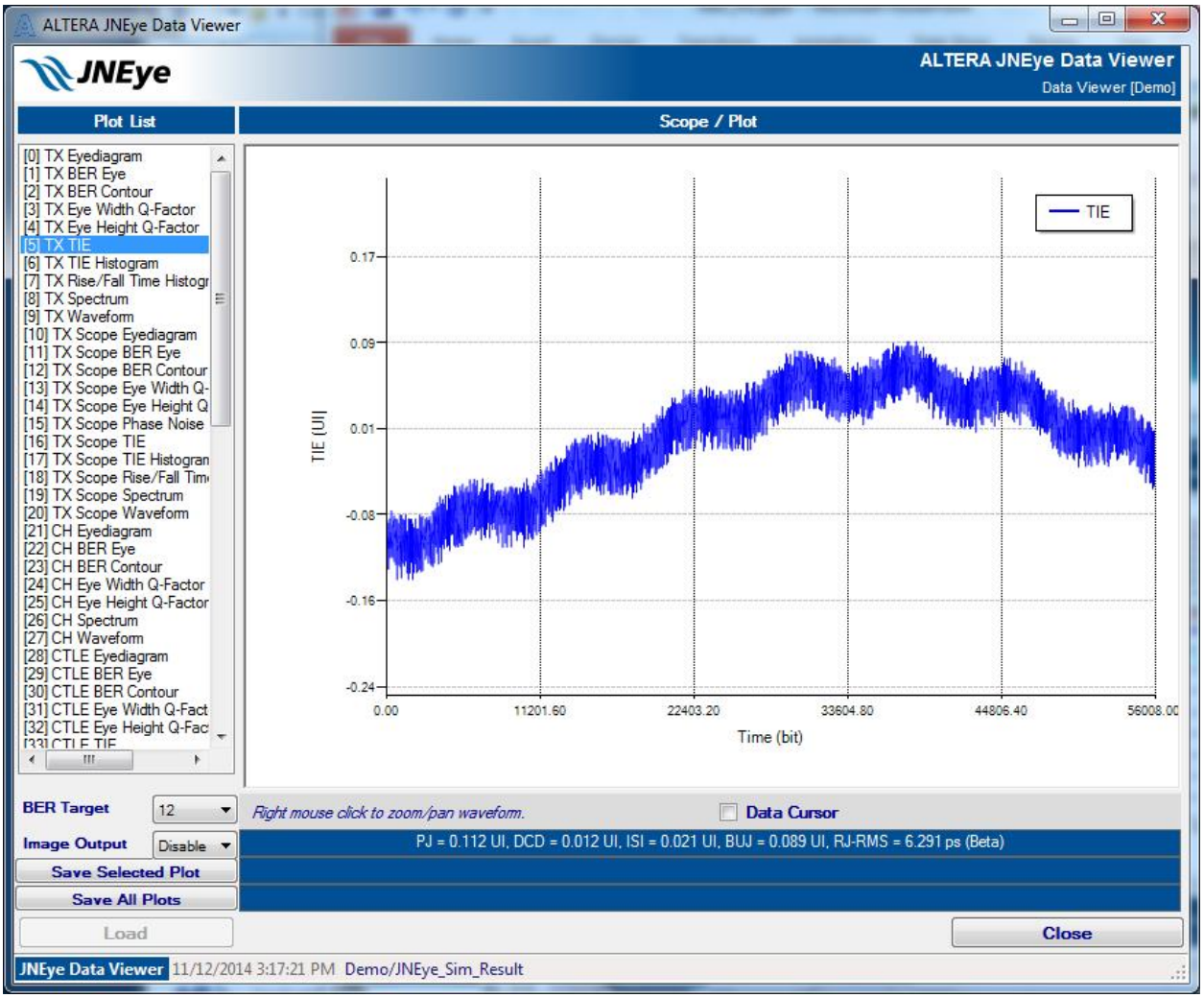
The CTLE setting is displayed for the test point after CTLE.

DFE coefficients are displayed for the test point after DFE.

Time Interval Error (TIE) Plots

TIE plots capture the time differences between the waveform transition time (across data sensing threshold) and ideal/reference waveform transition time. If **Jitter Analysis** is enabled and the simulation mode is **Hybrid**, jitter analysis results are displayed under the TIE plot.

Figure 2-73: Time Interval Error (TIE) Plot with Jitter Analysis Results



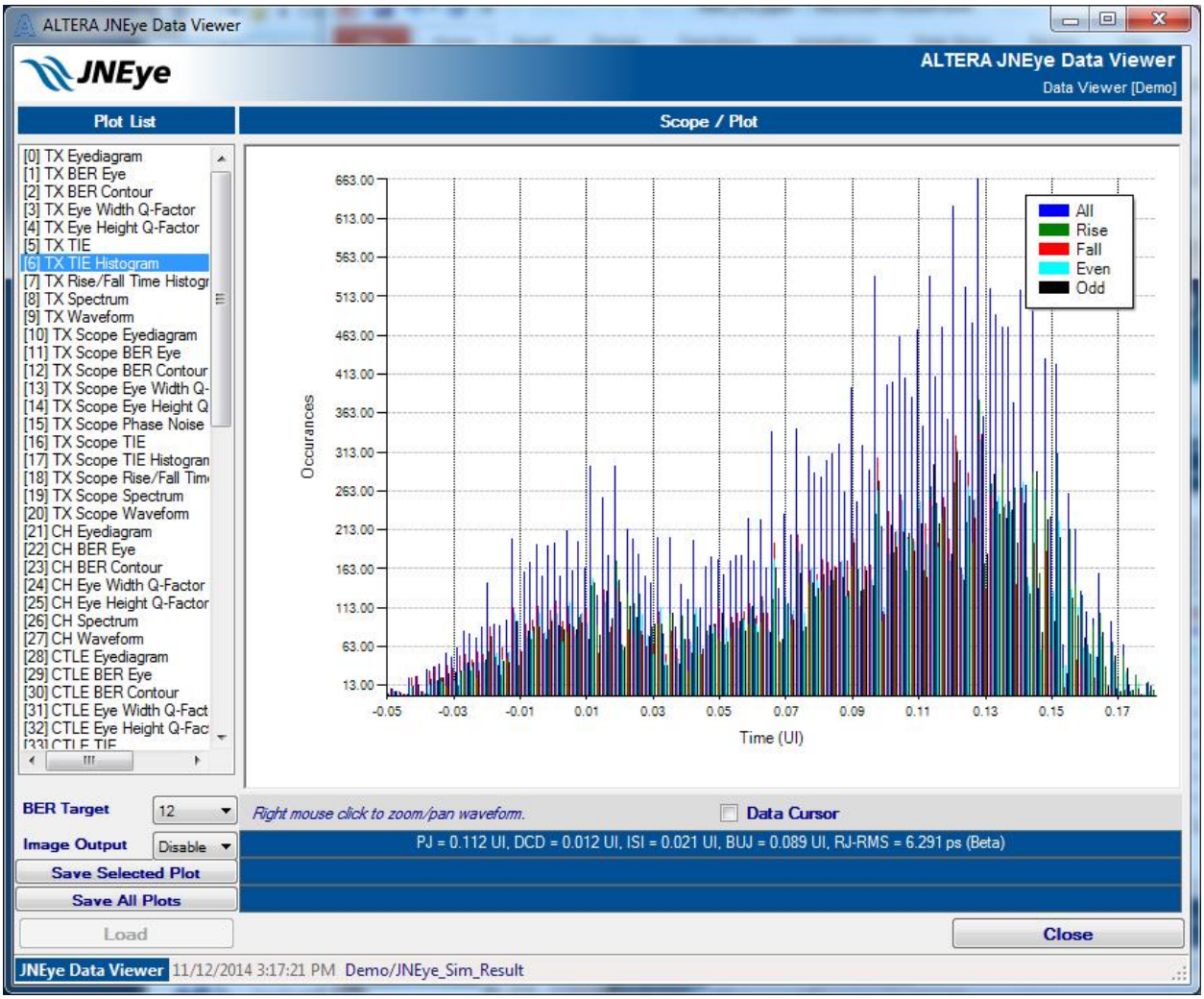
Time Interval Error (TIE) Histogram Plots

This plot shows the histogram of TIE records. Five histograms are displayed:

- All transitions
- Rising edge transitions
- Ffalling edge transitions
- Even bit edge transitions
- Odd bit edge transitions

If **Jitter Analysis** is enabled and the simulation mode is **Hybrid**, jitter analysis results are displayed under the TIE plot.

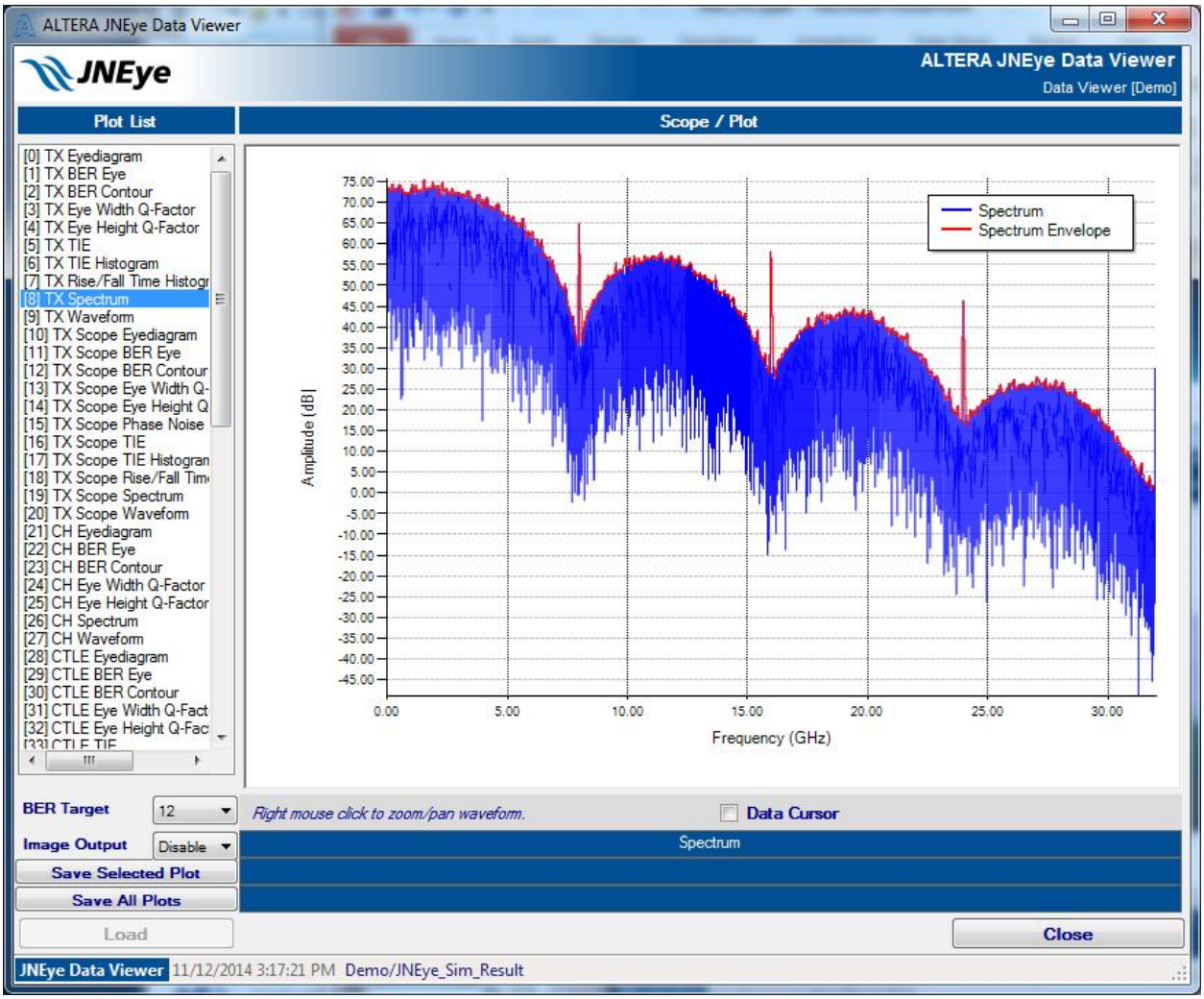
Figure 2-74: Time Interval Error (TIE) Histogram with Jitter Analysis Results



Waveform Spectrum Plots

The frequency spectrum of the waveform is plotted.

Figure 2-75: Waveform Spectrum Plot

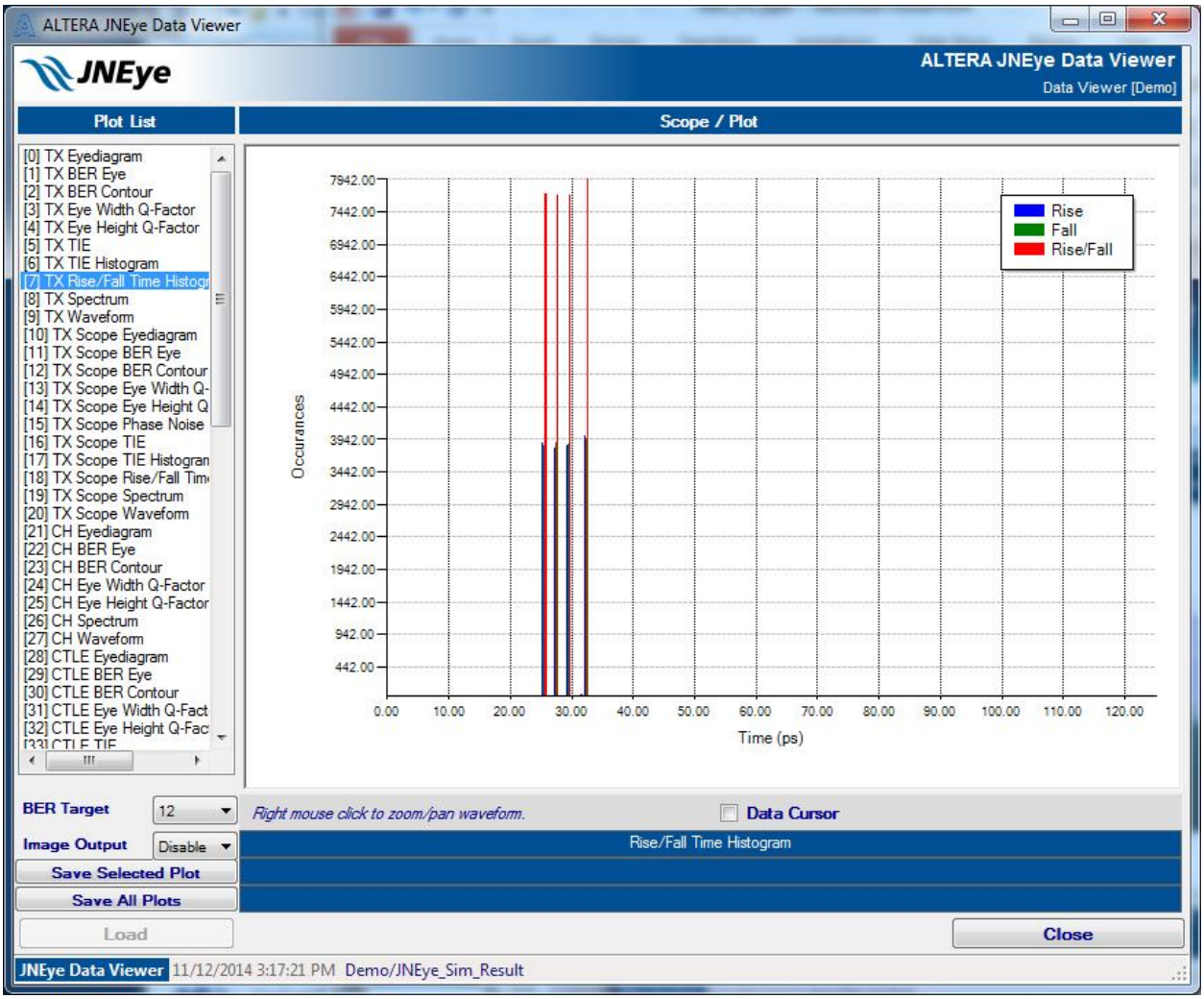


Rise/Fall Time Histogram Plots

JNEye calculates the rise/fall time across the bit time boundary.

Note: JNEye computes the rise/fall time based on the presented waveform. JNEye assumes there are no over- or under-shootings that are commonly seen when transmitter and receiver equalization effects are present. Furthermore, with a channel effect such as ISI, the waveform transition time may be slowed down dramatically compared to a transmitter output waveform. Therefore, you may see rise/fall times exceed the bit time boundary. You must use proper judgment when interpreting the rise/fall time results.

Figure 2-76: Rise/fall Time Histogram Plot



Waveform

For Hybrid mode or Full Waveform mode simulations, a waveform of each test point is plotted. The Data Viewer, by default, displays the final 4096 bits of the waveform. Use the following settings to specify the location of the waveform:

- **Plot**—The Plot menu specifies the reference location of the simulated waveform. It has the following choices:
  - **Beginning**—plots the waveform from the beginning of the simulation.
  - **End**—displays the last part of simulated waveform.
  - **Custom**—you specify the starting and ending bit locations.
- **Length**—If the **Plot** selection is **Beginning** or **End**, the length of waveform (in bits) to be plotted is specified.
- **From/to**—If the **Plot** selection is **Custom**, these two entries specify the start and end points of waveform (in bits) to be plotted.

Simulation Report

A simulation report is shown in the last page of the output windows. The simulation report is organized as follows:

- Simulation Log—If link optimization is performed, the link optimization FOM (figure of merit) transition is reported here.
- User-Defined Link Configuration—Link configuration is listed in this section which includes:
  - Transmitter Reference clock configuration
  - Transmitter configuration
  - Receiver configuration
  - Channel configuration
- Simulation Record—Report the simulation results at each test points
- Simulation Result Summary
  - TX-FIR/Pre-emphasis, RX CTLE, and DFE Settings
  - Eye Diagram Widths, Heights, and Margins to the eye diagram mask

```
------------------------------------------------------------
JNEye Simulation Log
Tue Apr 09 22:35:29 2013

Link Optimization Mode: TX = Manual, RX = Auto
Link Optimization FOM: Area

Link Optimization: Stage=Initialization

Altera JNEye Simulation Report
Tue Apr 09 22:35:44 2013
****************** User-Defined Link Configuration *********************
Project Name: Demo_7_SVGX_AVGZ_All
Simulation Mode: Hybrid

Data Rate: 10.3125 Gbps
Simulation Length: 65536 bits
Test Pattern: PRBS-23
BER Target: 1e-012

Transmitter Reference Clock:
            Frequency: 644.53 MHz
            Configuration Method: Option 2
                        Phase Noise Profile [Freq (Hz), Amplitude (dBc)]:
                  [1, -52]
                                    [10, -62]
                                    [100, -72]
                                    [1000, -82]
                                    [10000, -110]
                        Phase Noise Fmin: 100000 Hz
                        Phase Noise Fmax: 6.4453e+008 Hz
                        Spur Profile [Freq (Hz), Amplitude (dBc)]:
                                    [100000, -110]
                                    [1e+006, -90]
                                    [1e+007, -80]
                        Periodic Jitter:
                                    Method: Triangle
                                    Frequency: 0 Hz
                                    Amplitude: 0 ps
                        Hershey Key: 0.05
                        Sharkfin Key: 0.5

Transmitter: Stratix V GX
            Package: Stratix V GX
            VOD: 1 V
```

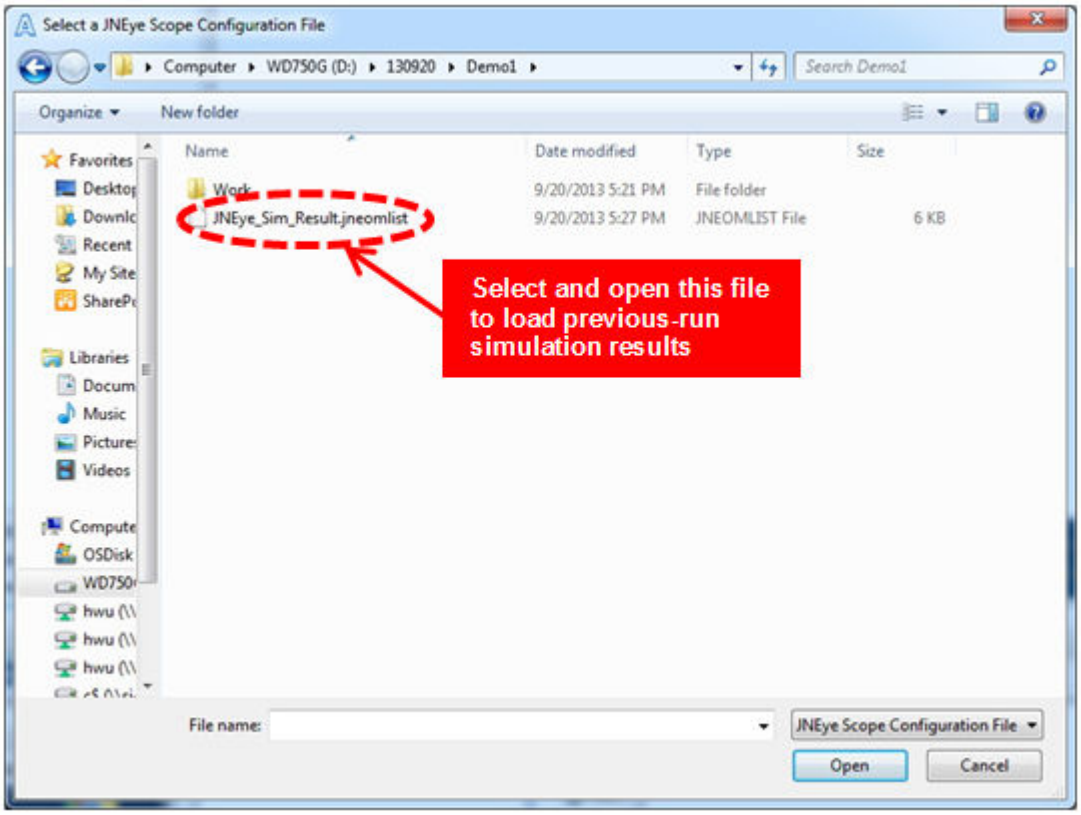
```
            PLL Type: Enable
            PLL Bandwidth: SVGX_TXPLL_High
            TX Pre-emphasis/FIR Mode: Off
            Jitter & Noise Configuration:
                        DJ    = 8.53333 ps
                        DCD    = 0 ps
                        BUJ    = 0 ps
                        RJ    = 0.74 ps-rms
                        SJ    = 0 ps at 0 MHz
                        DN    = 0 mV
                        BUN    = 0 mV
                        RN    = 0 mV-rms
Receiverr: Arria V GZ
            Package: Arria V GZ
            Supply Voltage: 1V
            CTLE Mode: Auto
            CDR Type: Alexander
            CDR Bandwidth: SVGX_CDR_Medium_BW
            DFE Enable: Enable
                        DFE Mode: Auto

Transmitter Jitter & Noise Configuration: No Jitter and Noise

Channel Configuration:
            [1] File Name: S12p_pin2pin_642010.s12p
                        Channel Type: Loss
                        Port Configuration: 2
                        Lane Number: 2
                        Port Number: 12
                        Aggressor ID: 1
                        Aggressor Relative Amplitude: 1
                        Aggressor Delay: 0

**************************************************************************

************************ Simulation Record ****************************
Transmitter Reference Clock    Random Jitter= 0 ps-RMS

Test Point 1 with Ideal Clock
            Stratix V GX TX Pre-emphasis: Pre-Tap 1 = 0.00 Post-Tap 1 = -0.00 Post-
Tap 2 = 0.00
            Eye Width=0.59UI (57.481ps), Eye Height= 789.36mV, Jitter(p-p)=0.41UI
(39.489ps)
            Random Jitter= 0.883382 ps-RMS

Test Point 1 with Recovered Clock
            Stratix V GX TX Pre-emphasis: Pre-Tap 1 = 0.00 Post-Tap 1 = -0.00 Post-
Tap 2 = 0.00
            Eye Width=0.74UI (71.875ps), Eye Height= 807.31mV, Jitter(p-p)=0.26UI
(25.095ps)
            Random Jitter= 0.840335 ps-RMS
            Bit Errors = 0

Test Point 2
            Eye Width=0.00UI ( 0.000ps), Eye Height=   0.00mV, Jitter(p-p)=1.00UI
(96.970ps)
            Random Jitter= 0.883382 ps-RMS

Test Point 3 with Ideal Clock
            CTLE Setting: Arria V GZ CTLE DC=0dB AC=12 (Gain=14.4111dB) BW=12GHz
Vod=H (Auto Mode, Method = Area)
            Eye Width=0.30UI (29.451ps), Eye Height= 146.21mV, Jitter(p-p)=0.70UI
(67.519ps)
            Random Jitter= 0.883382 ps-RMS

Test Point 3 with Recovered Clock
            CTLE Setting: Arria V GZ CTLE DC=0dB AC=12 (Gain=14.4111dB) BW=12GHz
```

```
Vod=H (Auto Mode, Method = Area)
            Eye Width=0.41UI (39.867ps), Eye Height= 182.92mV, Jitter(p-p)=0.59UI
(57.102ps)
            Random Jitter= 0.784156 ps-RMS
            Bit Errors = 0

Test Point 4 with Ideal Clock
            DFE Coefficients = [     0,     1,    -1,     0,     0,]
            Eye Width=0.34UI (33.049ps), Eye Height= 157.31mV, Jitter(p-p)=0.66UI
(63.920ps)
            Random Jitter= 0.883382 ps-RMS

Test Point 4 with Recovered Clock
            DFE Coefficients = [     0,     1,    -1,     0,     0,]
            Eye Width=0.50UI (48.485ps), Eye Height= 187.33mV, Jitter(p-p)=0.50UI
(48.485ps)
            Random Jitter= 0.784156 ps-RMS
            Bit Errors = 0

*******************************************************************************
******************

Simulation Result Summary

********** TX-FIR/Pre-emphasis, RX CTLE and DFE Settings ************
Pre-emphasis      :Pre-tap1          main-tap          Post-tap1          Post-
tap2
            Levels         :0.000             0.000             0.000
0.000
            Coeff          :0.000             1.000             0.000
0.000
CTLE Setting      :DC = 0.000 dB, AC = 12.000,  BW = 12.000, Volt = 1.000
CTLE AC Gain      :14.411 dB
DFE                  :tap1              tap2              tap3
tap4          tap5
            Levels         :0.000             1.000             -1.000
0.000            0.000
            Coeff          :0.000             0.036             -0.036
0.000            0.000
*******************************************************************************
***************************

********** Eye Diagram Width and Eye Diagram Height ******************
                               Eye Width       Eye Height       Eye Opening
                               [UI]              [V]                Area [UI*V]
TX Output (Scope)            :0.7412           0.8073              0.5984
TX Output                       :0.5928           0.7894              0.4679
Channel Output               :0.0000           0.0000              0.0000
CTLE Output (Retimed)        :0.4111           0.1829              0.0752
            Eye Mask Margin        :0.1018           0.1129
CTLE Output                     :0.3037           0.1462              0.0444
            Eye Mask Margin        :-0.0057          0.0762
DFE Output (Retimed)         :0.5000           0.1873              0.0937
            Eye Mask Margin        :0.1906           0.0973
DFE Output                      :0.3408           0.1573              0.0536
            Eye Mask Margin        :0.0314           0.0673
*******************************************************************************
***************************

Simulation Time: 0:1:6

Overall Simulation Time: 0:1:21
-------------------------------------------------------------------
```

Use the Data Viewer to see previous JNEye simulation results by clicking **Load**. A file browser opens and helps you find the master JNEye output data file (**JNEye_Sim_Result.jneomlist**) for individual

simulations. JNEye simulation output data is usually located in a file directory that has the same name as the saved project name. For example, if the saved JNEye configuration file is **Demo1.jne**, the previous simulation results are stored a directory named "Demo1". Navigate to the directory, select the **JNEye_Sim_Result.jneomlist** file, and open it to load the simulation data.

Figure 2-77: Load Previous JNEye Simulation Results



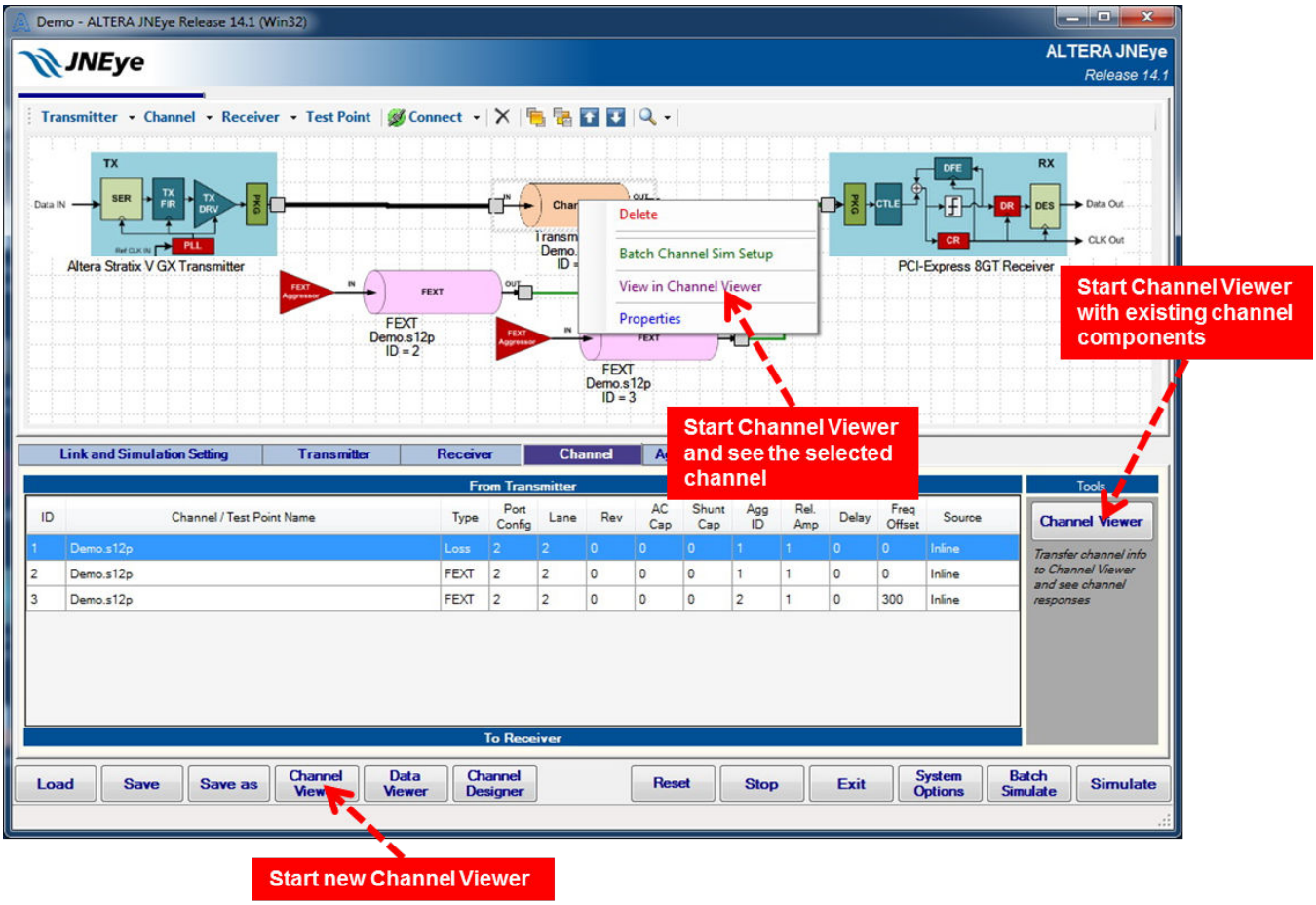
JNEye Channel Viewer Module

The JNEye Channel Viewer provides a convenient way of observing and comparing channel characteristics. The following types of channel characteristics, which are represented by Touchstone S-parameter format, can be displayed in the Channel Viewer:

- Standard-mode / Single-ended S-parameter—for example, S_{11}, S_{12}, S_{21}
- Mixed-mode / Differential S-parameters—for example: S_{dd11}, S_{dd21}, S_{cd21}
- Frequency Domain Plots: Amplitude and propagation/group delay plots
- Time Domain Plots: Impulse responses and single-bit responses

Channel Viewer also provides channel compliance checks and channel analysis. Use these features to observe a channel's characteristics and its associated signal integrity matrices.

Figure 2-78: Start JNEye Channel Viewer from JNEye Controller Module

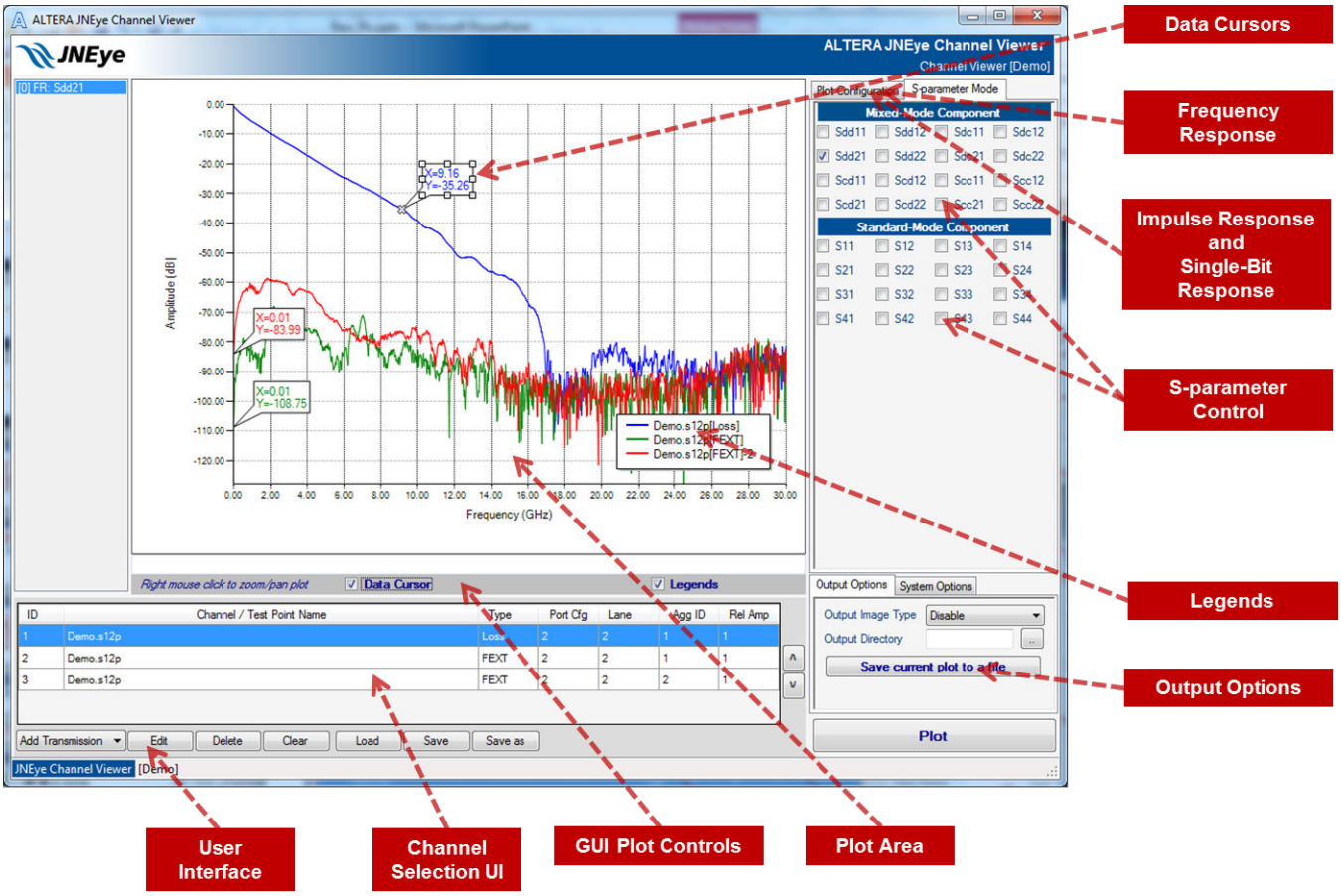


There are four ways to start JNEye Channel Viewer:

- Double-click the **JNEye_Channel_Viewer_SA.exe** icon in Windows Explorer.
- Click **Channel Viewer** in the JNEye Control Module to start a new Channel Viewer (refer to the previous figure).
- Click **Channel Viewer** in the JNEye Control Module's **Channel** tab (refer to the following figure). When you start JNEye Channel Viewer from the **Channel** tab, the channel information from the link configuration is transferred to the Channel View and is ready for viewing.
- Select a channel in JNEye Control Module's Link Designer, right-click, and select **View in Channel Viewer**.

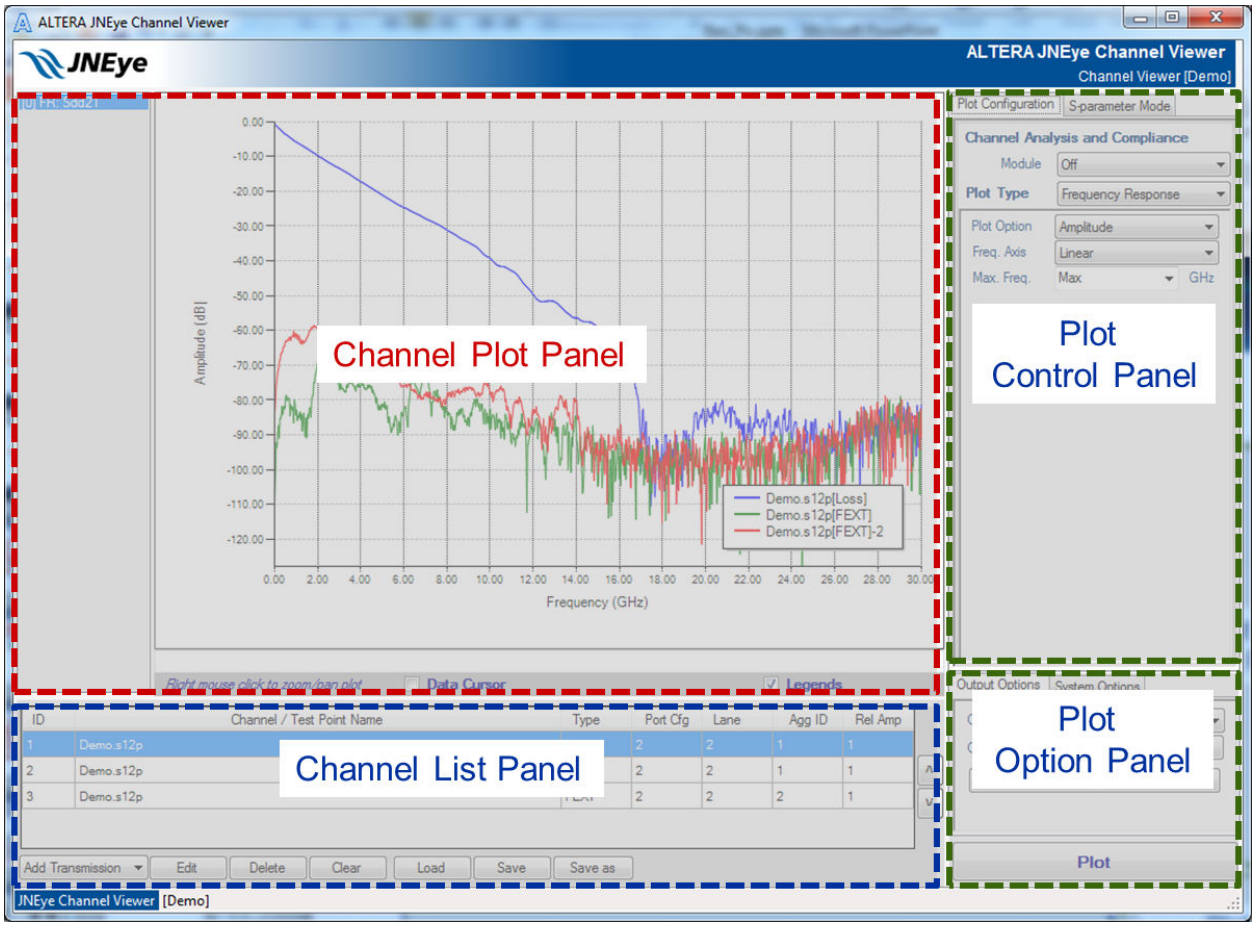
The following figure shows the JNEye Channel Viewer user interface. The viewer has six panels that allow you to select and control the channel plot options.

Figure 2-79: JNEye Channel Viewer User Interface



The following figure shows the Channel Viewer GUI panel partitions.

Figure 2-80: JNEye Channel Viewer GUI Panel Partitions



Channel Plot Panel

This panel contains the Channel Viewer and Plot Selector. The JNEye Channel Viewer shows the characteristics of the channels in the channel list with the plot options specified. Use the Channel Viewer to plot channels with different options and browse the plots. Use the Plot Selector to choose one of the existing plots.

The Channel Viewer provides the following GUI capabilities:

- **Zoom In**, **Zoom Out**, **Pan**, **Data Select**—Right-click on the Channel Plot panel to select one of these functions. To zoom in on the plot, select **Zoom In** and then click and drag a rectangle box to show the details of the plot. To zoom out, select **Zoom Out**. Up to ten previous scalings are saved, so you can restore older versions by clicking **Zoom Out** more than once. To pan over the plot, select **Pan** and then click and drag the plot.
- **Data Cursor**—By checking the **Data Cursor** radio button, the data cursor boxes will show. You can select and drag a data cursor box with the data values shown in the box. The data values are colored according to the data lines.
- **Legends**—Plot legends are shown when plots are generated. Use the **Page-Up**, **Page-Down**, **Home**, and **End** keys on the keyboard to move the legend box. You can also check or uncheck the **Legends** check box to show or hide the legend box.

Channel List Panel

This panel maintains the channels of interest. Channels can be either transferred from the JNEye Control Module or added within the Channel Viewer. The channel list in the Channel Viewer is independent from the list in JNEye Control Module. Therefore, you can add and delete channels in the Channel Viewer without affecting the lsimulation configuration in the JNEye Control Module.

An S-parameter channel component, such as a connector, cable, or backplane, can be described by the following parameters or information as shown in the Channel List:

- **ID**—Sequence or location of the channel component.
- **Channel Name**—An S-parameter file that describes the channel component. The S-parameter file can be 4-port, 8-port, 12-port, 16-port, and so forth.
- **Type**—Specify the type of **channel characteristics** in the link simulation. The type of channel characteristics can be insertion loss (**Loss**), far-end crosstalk (**FEXT**), or near-end crosstalk (**NEXT**). Change the channel type by selecting the channel from the channel list and then selecting the appropriate channel type from the Type menu.
- **Port Configuration** (Port Cfg)—Depending on the S-parameter measurement condition, the port configuration can be one of the types shown in the following figures. You can change the port configuration of an S-parameter by using the menu below the Port Configuration list box.

Figure 2-81: S-parameter with Port Configuration—Type 1

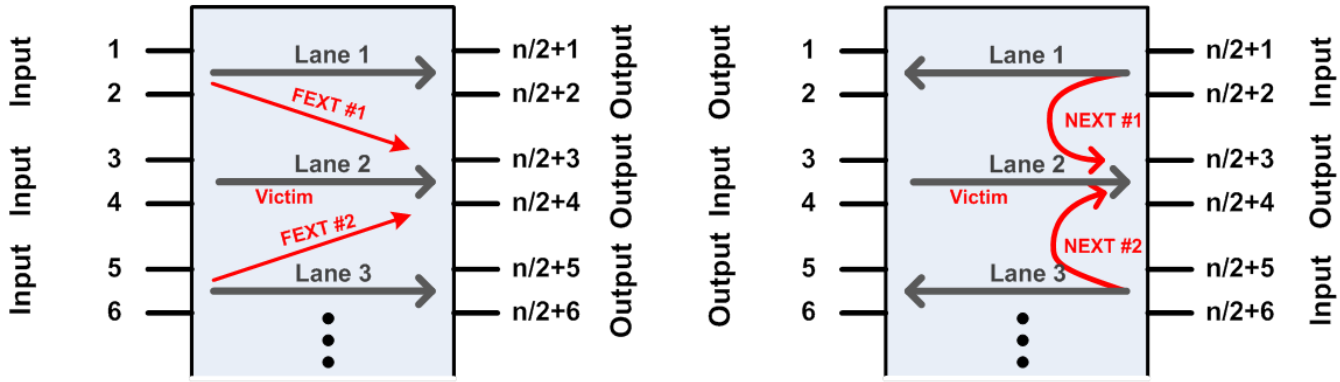


Figure 2-82: S-parameter with Port Configuration—Type 2

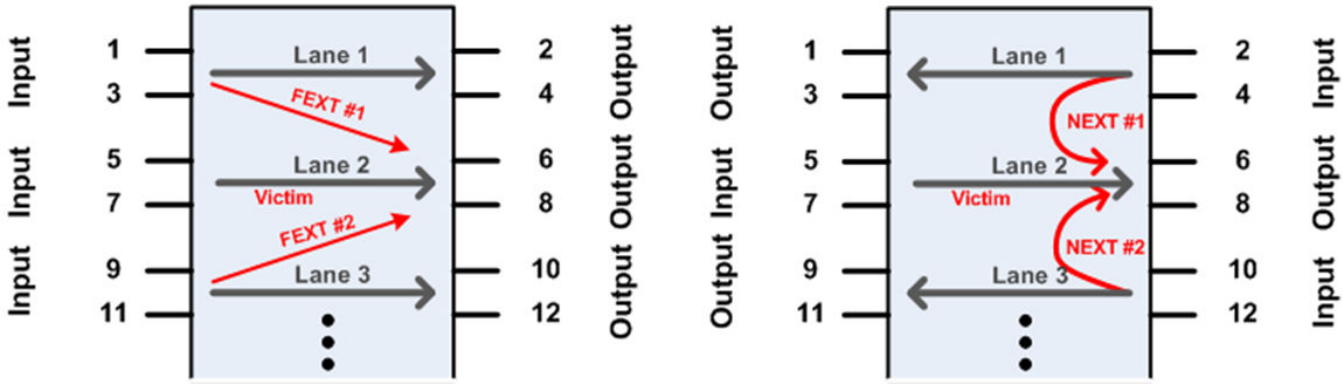


Figure 2-83: S-parameter with Port Configuration—Type 3

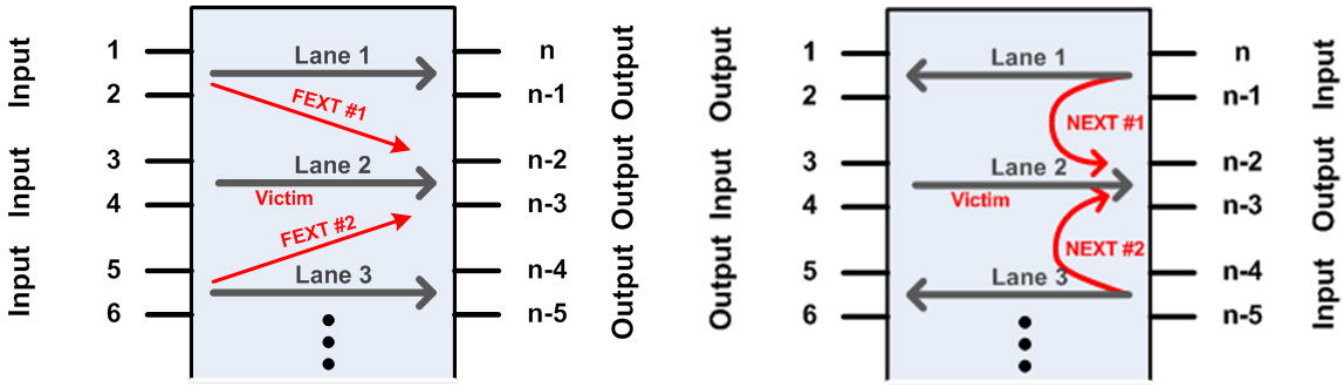
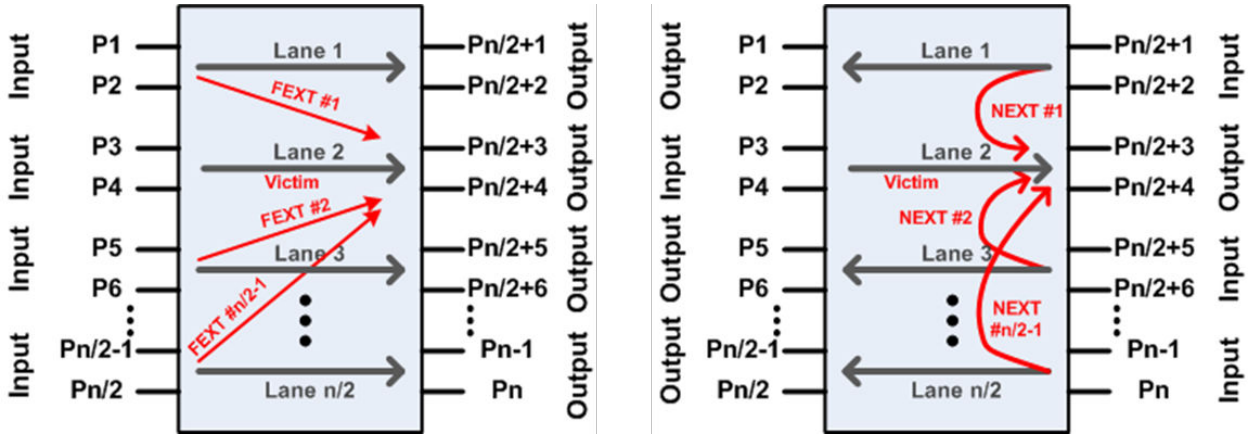


Figure 2-84: S-parameter with Custom Port Configuration



- **Lane ID** (Lane)—For multiple channel/lane S-parameters (8-port and above) a channel/lane must be chosen for link simulations. For example, the above figures show a 12-port 3-lane S-parameter. After loading the channel file, JNEye assigns the middle lane as the default simulating channel (or victim channel for crosstalk simulations). You can change the Lane ID by using the menu below the Lane ID list box. For 2-port or 4-port S-parameter models, the Lane ID is ignored.
- **Aggressor ID** (Agg ID)—For multiple channel/lane S-parameters simulating crosstalk effects, you must specify the aggressor location. For example, the above figures show four possible crosstalk configurations from a 12-port S-parameter model. Use the menu below the Aggressor ID list box to change the aggress location. For Victim channel (Loss type), the Aggressor ID field is ignored.

  Note: The Aggressor ID is indexed in a way that excludes the victim lane. For example, in a 12-port S parameter, there are three lanes. The middle lane (Lane ID 2) is the victim lane. The two aggressor channels have Aggressor IDs 1 and 2, not 1 and 3.
- **Relative Amplitude** (Rel Amp)—You can manually adjust the amplitude of crosstalk (NEXT/FEXT) channel components. The amplitude adjustment is reflected in the channel plots and the channel compliance results. The amplitude adjustment is in a linear scale.

The Channel List Panel contains the following command buttons:

- **Add Channel**—Open a file browser and locate the required channel model files.
- **Delete**—Delete a channel or test point.
- **Duplicate**—Duplicate the selected channel component or test point in the channel list.
- **Disable**—Disable the selected channel component or test point.
- **Enable**—Enable the selected channel component or test point.
- **Clear**—Delete all channel components and test points.
- **Load**—Load channel list and channel viewer configuration.
- **Save**—Save current channel list and channel viewer configuration.
- **Save as**—Save current channel list and channel viewer configuration in a new configuration file .
- **Move Up** (/\)—Move the selected channel component or test point up toward the transmitter side.
- **Move Down** (\/)—Move the selected channel component or test point down toward the receiver side.

Plot Option Panel

The Plot Option panel has the following sub-panels:

- S-parameter mode panel
- Plot configuration panel

S-parameter Mode Panel

Figure 2-85: S-parameter Mode Panel

- **Mixed-Mode Selector Panel**—This panel allows you to select and plot an S-parameter's mixed-mode characteristics. The JNEye Channel Viewer can convert standard-mode (that is, single-ended) frequency responses into its differential–pair format (mixed-mode) frequency responses. For high-speed serial links with differential signaling scheme, Altera recommends you observe channel characteristics and performance in mixed-mode.
- **Standard-Mode Selector Panel**—This panel allows you to select and plot an S-parameter's standard-mode characteristics. An open 4-port single-ended S-parameter is supported in this plot mode.

Plot Configuration Panel

The **Channel Analysis and Compliance Module** menu controls the channel characteristics plotting modes:

- **Off**—Channel Viewer plots channel characteristics as directed by user configuration. In the mode, you can plot frequency responses, impulse responses, and single bit responses. This is the default Channel Vierwer plotting mode.
- **Channel Analysis**—Channel Viewer performs a sequence of operations to calculate and show channel performance in terms of ILD (Insertion Loss Deviation), RL (Return Loss), ICR (Insertion Loss to Crosstalk Ratio), and Crosstalk Noise calculations. This allows you to determine the wellness of the channels.

  Channel Analysis supports customizable compliance masks for IL, ILD, RL, ICN, and ICR. This feature can be used to perform custom channel compliance checks for proprietary links. When **Custom** is selected, you can enter channel compliance mask definition in each text box with the format: frequency (Hz) and amplitude (dB). You can also load a predefined custom channel compliance mask definition from a file.
- **10GBASE-KR** Channel Compliance—Channel Viewer performs channel compliance checks per 10 Gbps Ethernet over backplane (IEEE 802.3ap, 10GBASE-KR) standards.
- **OIF CEI-28G-SR 3.0** Channel Compliance—Channel Viewer performs channel compliance checks per OIF CEI-28G-SR 3.0 standards.
- **OIF CEI-25G-LR 3.0** Channel Compliance—Channel Viewer performs channel compliance checks per OIF CEI-25G-LR standards.
- **OIF CEI-28G-MR 3.1** Channel Compliance—Channel Viewer performs channel compliance checks per OIF CEI-28G-MR standards.

User-Directed Channel Plotting

Figure 2-86: Plot Configuration Panel (Frequency Response)

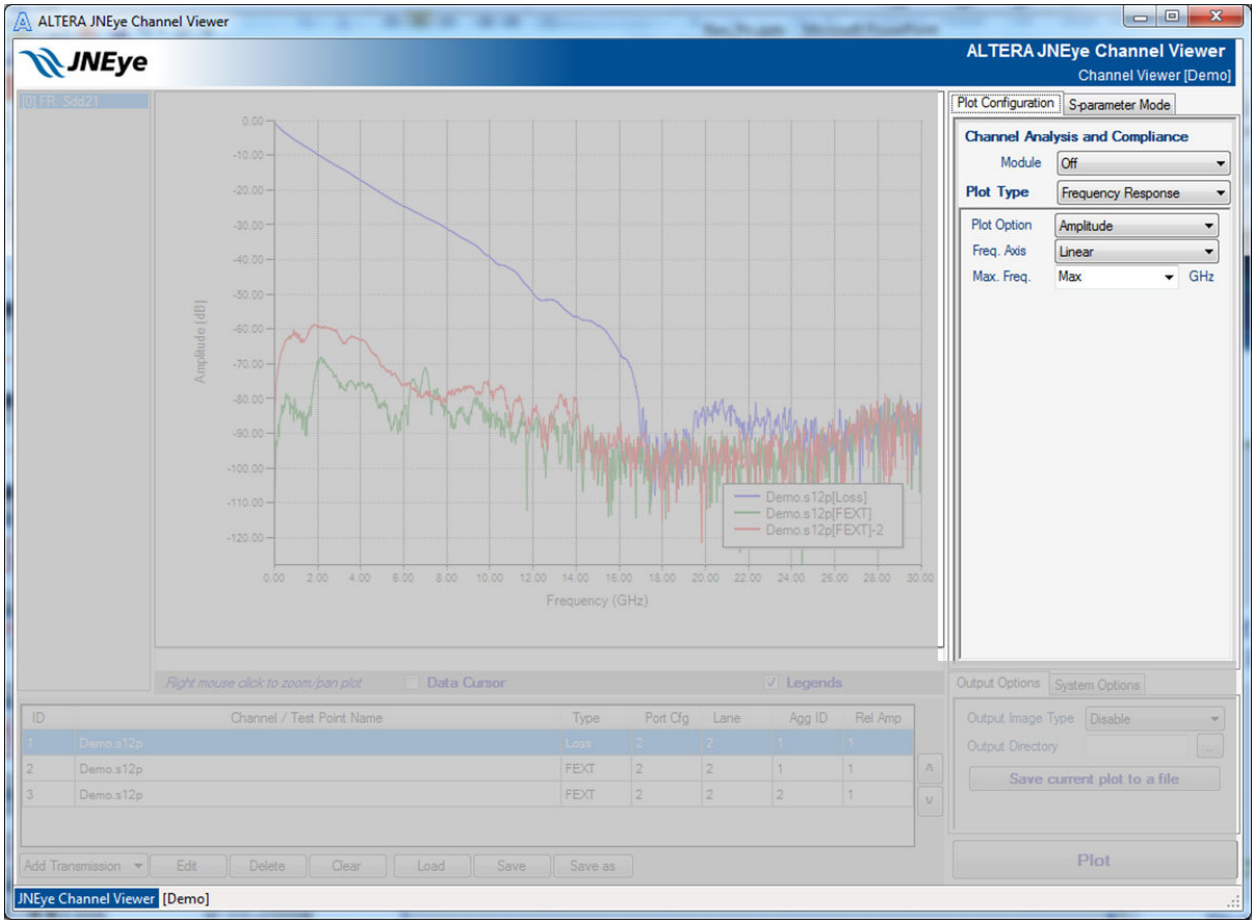
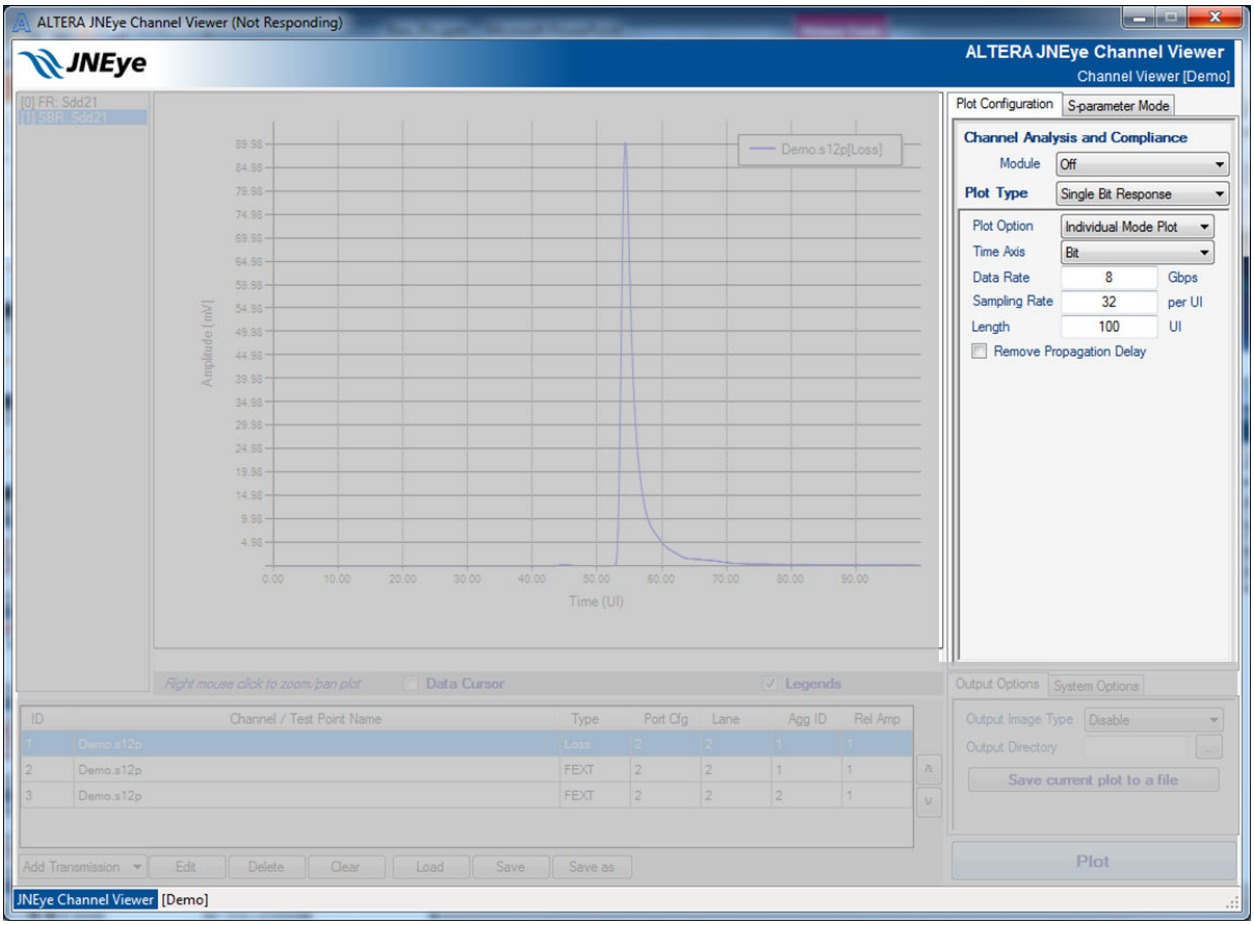
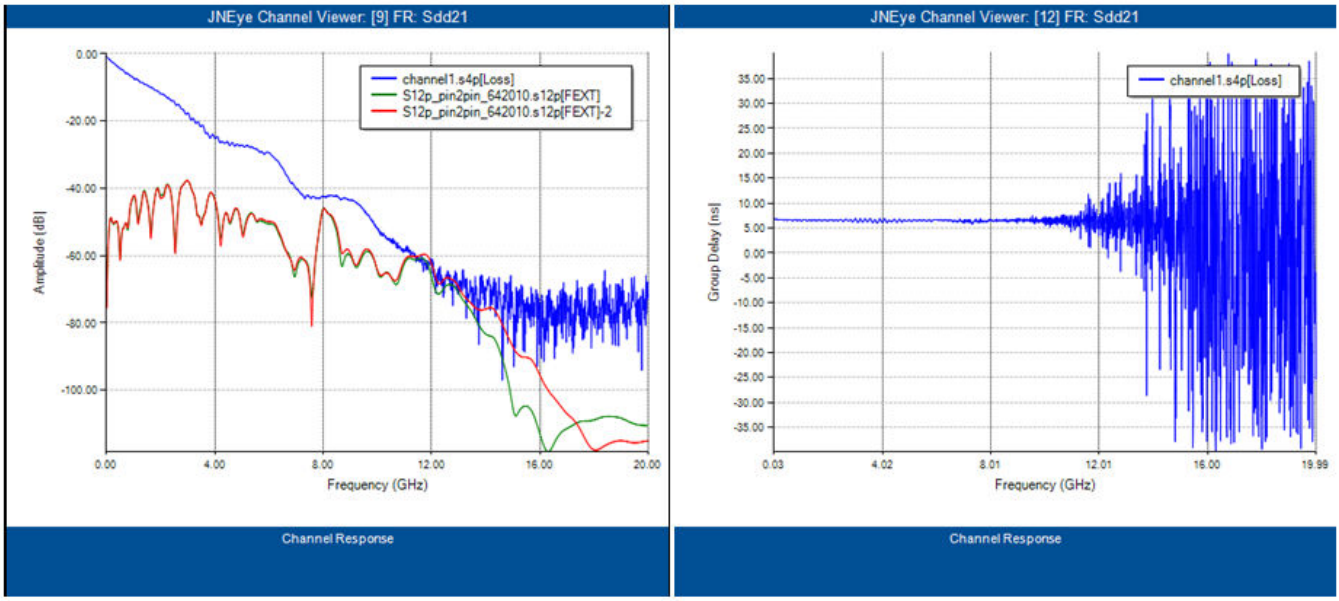


Figure 2-87: Plot Configuration Panel (Impulse Response and Single Bit Response)



This panel allows you to select and configure the channel plotting. The JNEye Channel Viewer can plot channel characteristics in either frequency domain or time domain. Typical frequency domain amplitude and group delay plots are shown in the following figure.

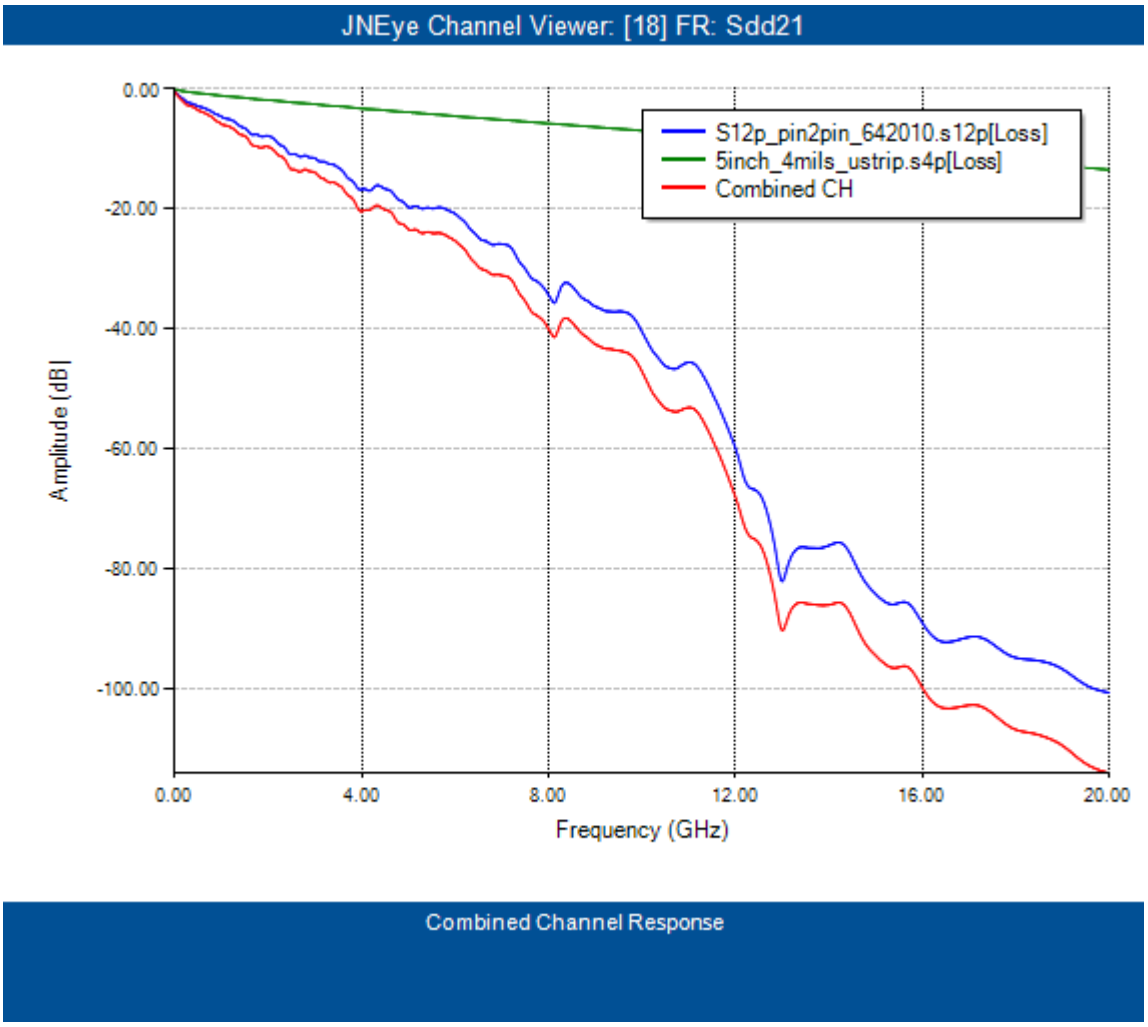
Figure 2-88: Typical Frequency Domain Channel Characteristics Plots



The JNEye Channel Viewer plots the channels' amplitude and group delay frequency responses in a linear or logarithmic frequency scale. It also allows you to limit the plot frequency range. When multiple transmission channels (such as loss or victim) are in the Channel List, you can plot the cascaded channel response by turning on the **Plot Combined Channel Response** option in the **Systems Options** panel. An example of a combined channel response is shown in the following figure, in which a lossy backplane channel is cascaded with a 5" microstrip PCB trace.

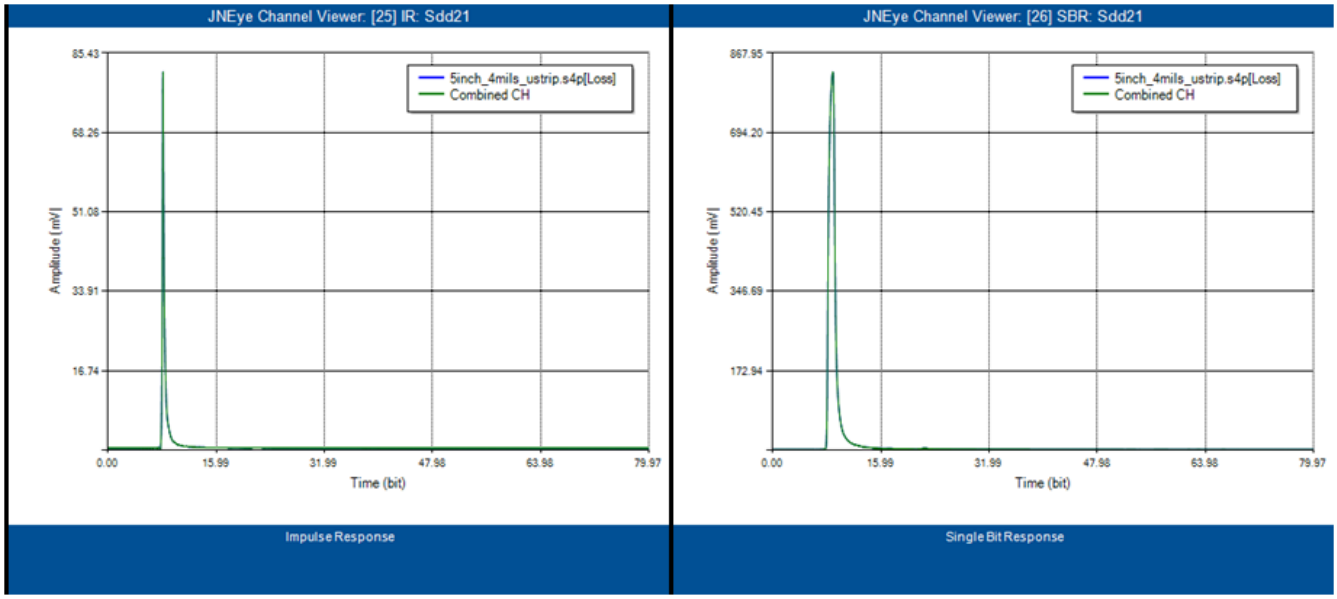
Note: JNEye only cascades or combines victim transmission channels. Crosstalk channels are not combined (with the loss channels) in the plot.

Figure 2-89: Combined Channel Response Example



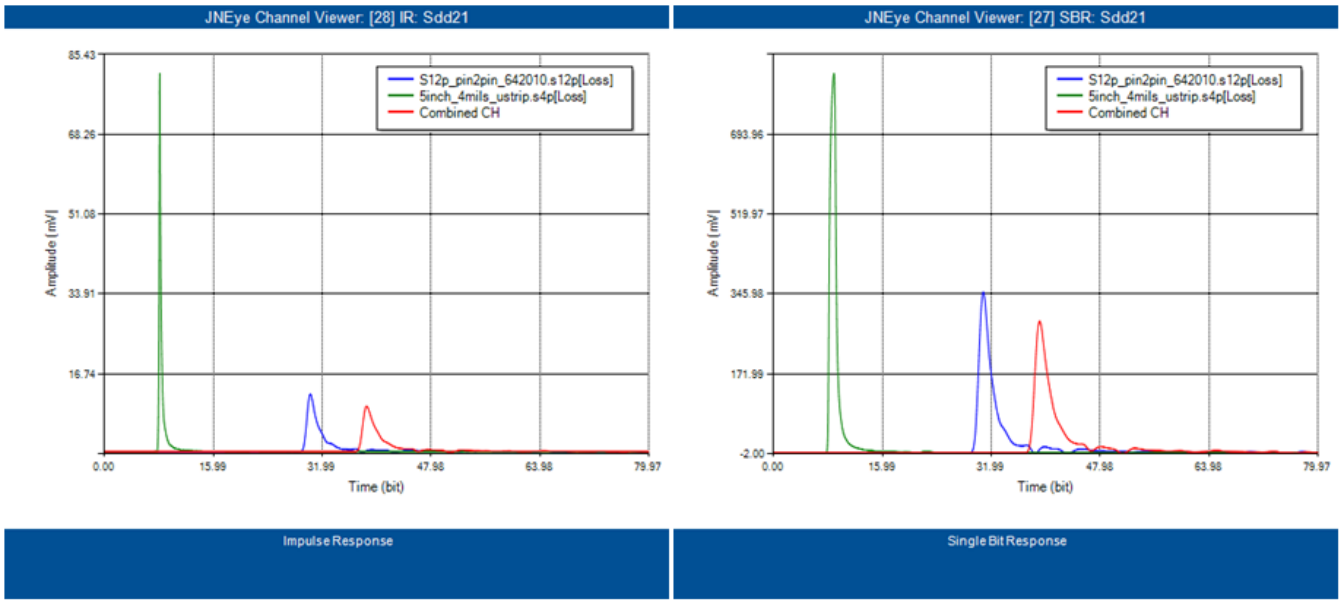
The JNEye Channel Viewer can also plot channel responses in a time-domain. It can compute the impulse response (IR) and single-bit response (SBR) of a channel or a combined response of channels. When performing a time-domain plot, you must specify the maximum frequency and plot length of the time-domain response. The following figure shows examples of impulse response and single-bit response of a 5” microstrip PCB trace.

Figure 2-90: Impulse Response and Single-Bit Response Examples



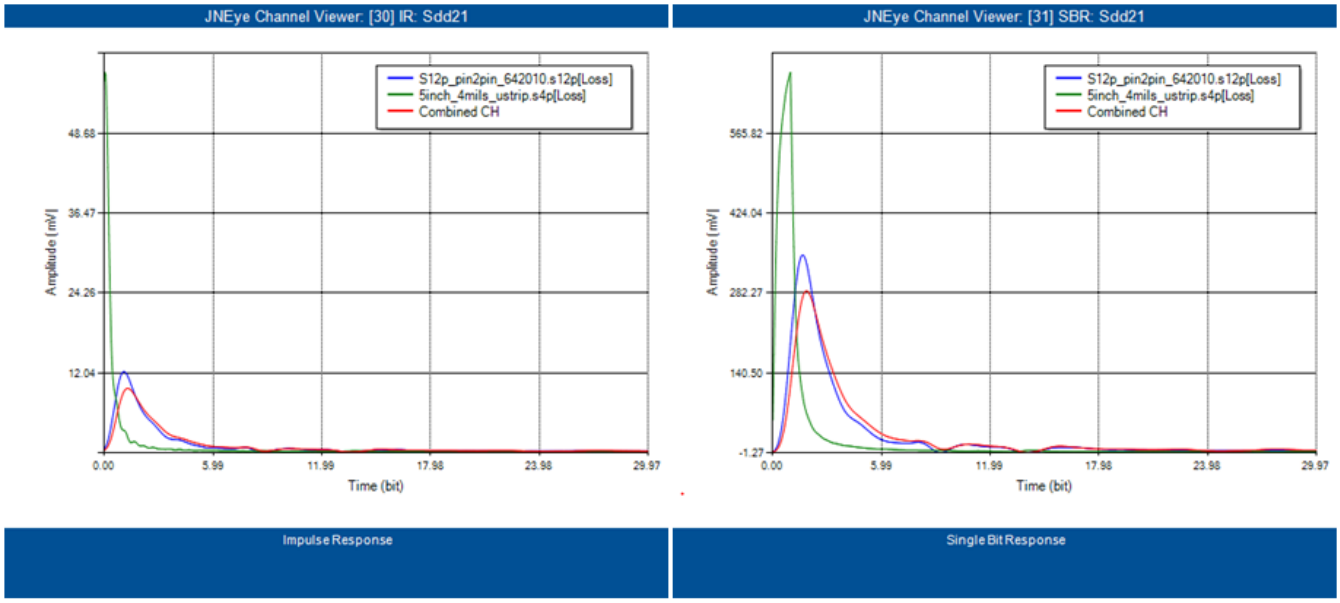
Combined time-domain channel responses can also be done in the JNEye Channel Viewer. The following figure shows examples of combined time-domain channel response of a lossy backplane channel and a 5" microstrip PCB trace.

Figure 2-91: Combined Time-Domain Channel Responses



By turning on the **Remove Propogation Delay** option, the JNEye Channel Viewer can mathematically remove the delay of channels so that more direct comparison among channels can be seen. The following figure shows an example of "Remove Propogation Delay" channel response of the same channels used in the previous figure.

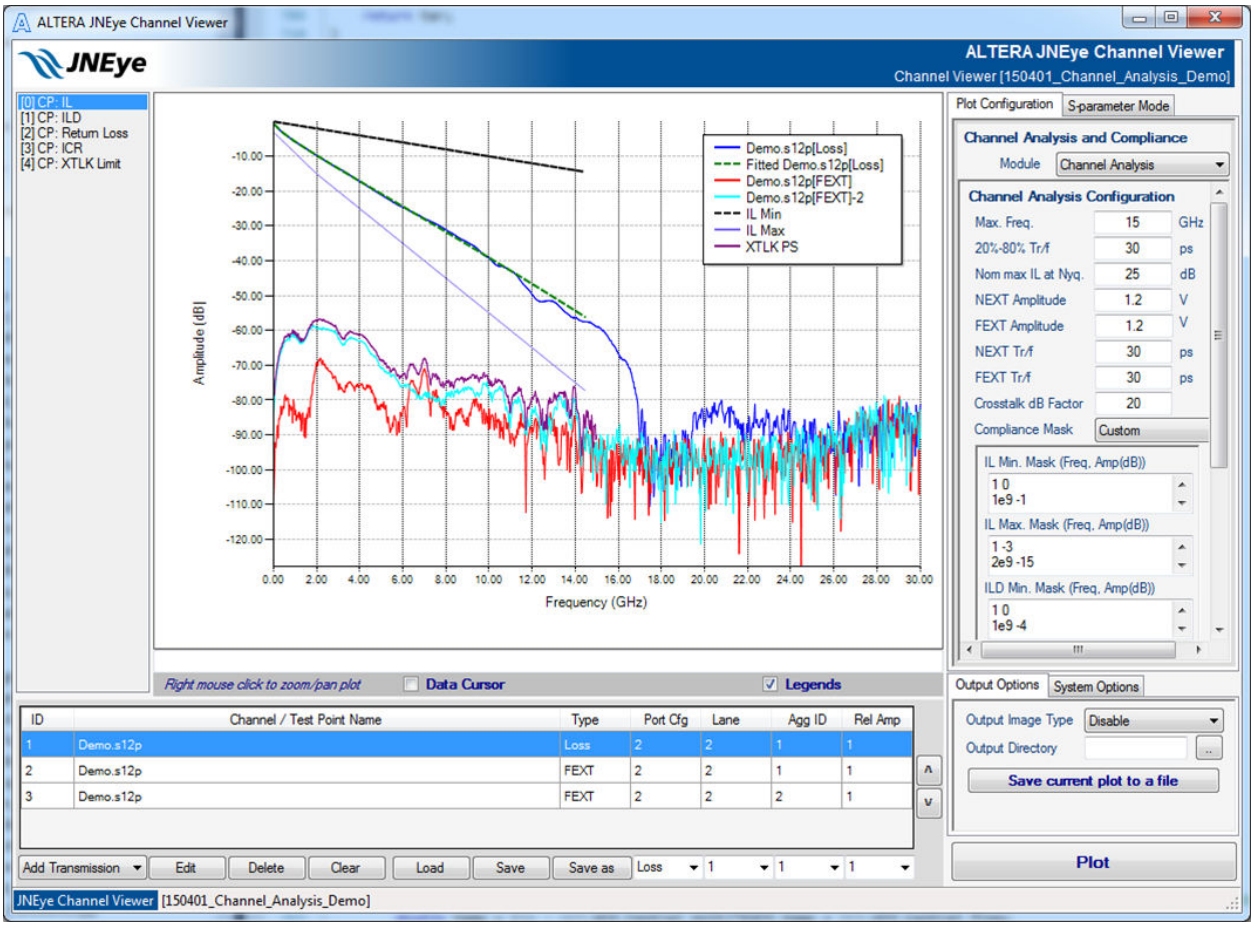
Figure 2-92: Time-Domain Channel Plots with "Remove Propogation Delay" Option



Channel Analysis

The following figure shows the Channel Analysis GUI.

Figure 2-93: Channel Analysis User Interface



In the Channel Analysis Configuration panel, the following parameters can be configured to your link configuration or preferences:

- **Max. Freq.**—Maximum frequency where channel analysis will be performed
- **20%-80% Tr/Tf**—20%-80% rise/fall time of the input signal to the victim or transmission channel(s)
- **Nom max IL at Nyquist**—Nominal maximum insertion loss at Nyquist frequency. This parameter specifies the maximum allowed insertion loss at Nyquist frequency, which is defined as half of the maximum frequency specified above.
- **NEXT Amplitude**—Near-end crosstalk aggressor signal amplitude
- **FEXT Amplitude**—Far-end crosstalk aggressor signal amplitude
- **NEXT Tr/Tf**—Near-end crosstalk aggressor 20%-80% rise/fall time

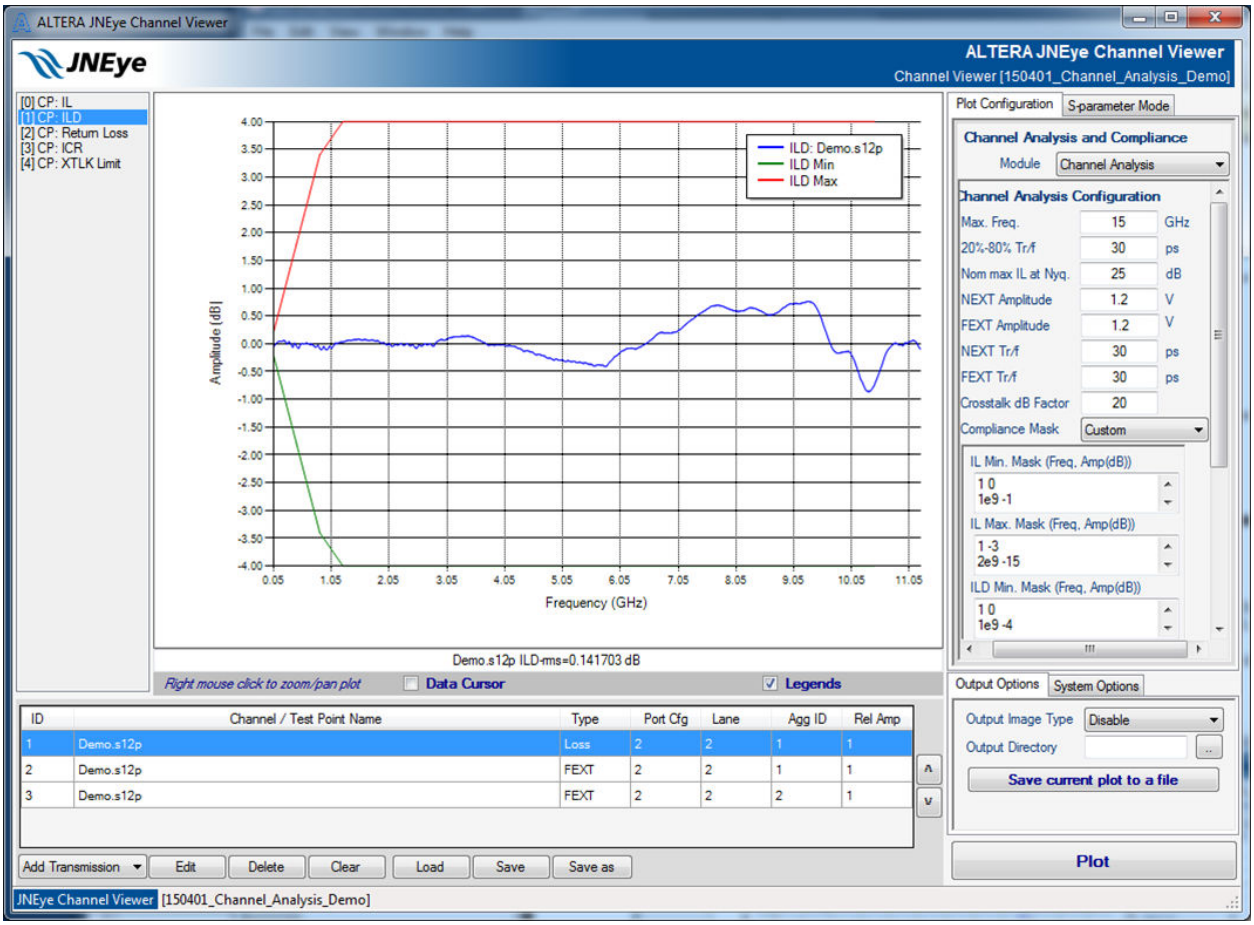
- **FEXT Tr/Tf**—Far-end crosstalk aggressor 20%-80% rise/fall time
- **Crosstalk dB Factor**—This parameter, Y, defines how dB is calculated where dB = Y*log10(amplitude)
- **Compliance Mask**—Select the channel compliance mask to be used in the channel analysis. The **Compliance Mask** menu contains the following selections:
  - **10GBASE-KR**—Use the 10GBASE-KR channel compliance mask.
  - **OIF CEI-28G-SR 3.0**—Use the OIF CEI-28G-SR channel compliance mask.
  - **OIF CEI-25G-LR 3.0**—Use the OIF CEI-25G-LR channel compliance mask.
  - **Custom**—Refer to **Figure 2-93**. Several text boxes for each channel compliance check item are shown. You can copy or manually input the mask definitions. The format for each mask definition data point is “Frequency (in Hz)", followed by "Amplitude (in dB)”. The number of data points is limited to the maximum text length allowed by the text box (the maximum size is 32767 bytes). The frequency grid of a mask must be monotonic increasing.
  - **Load from file**—Allows you to load a predefined custom channel compliance. Each mask definition starts with a keyword, followed by a pair of numbers that represent the data points for “Frequency (Hz)" and "Amplitude (dB)”. Following is a sample of a custom channel compliance mask file:

```
IL Mask Min
1 0
1e9 -1
10e9 -2.5
IL Mask Max
1 0
1e9 1
10e9 2.5
ILD Mask Min
1 0
1e9 -4
10e9 -4
ILD Mask Max
1 0
1e9 4
10e9 4
RL Mask
1 -10
1e9 -10
10e9 -4
ICR Mask
1e9 55
25e9 25
ICN Mask
1 10
5 10
25 0
```

When you click **Plot**, the Channel Viewer computes and generates a sequence of plots that show the performance of the channels in the channel list

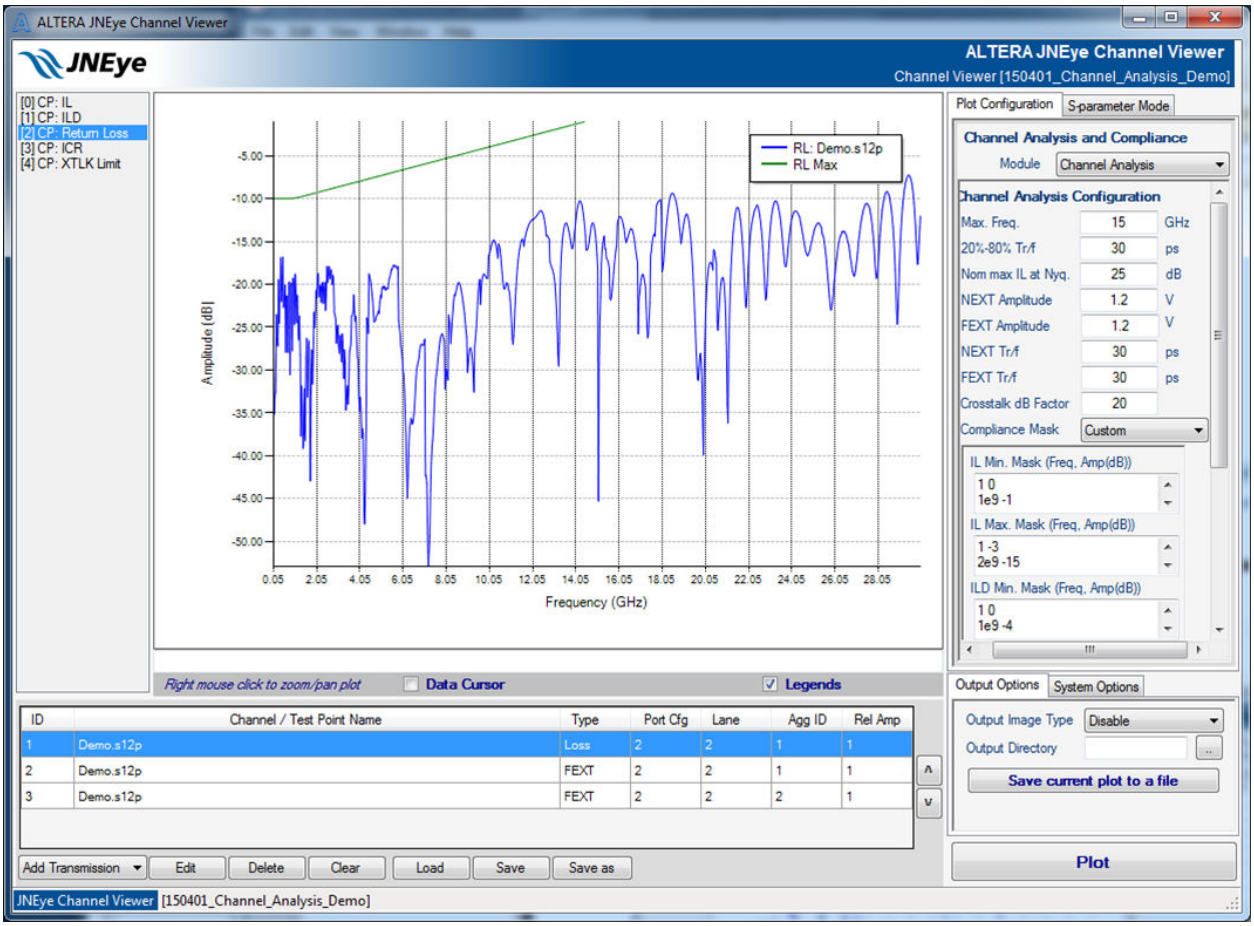
- **Insertion Loss** Plot—This plot is labeled **CP: IL**. In this plot, the insertion loss of channels, fitted curve of transmission channels’ insertion loss, crosstalk channels’ amplitude, and power sum of all crosstalk channels is shown. An example is illustrated in the above figure.
- **Insertion Loss Deviation** Plot—This plot is labeled **CP: ILD**. In this plot, the insertion loss deviation is shown, as in the following figure.

Figure 2-94: Channel Analysis Module's Insertion Loss Deviation (ILD) Analysis Example



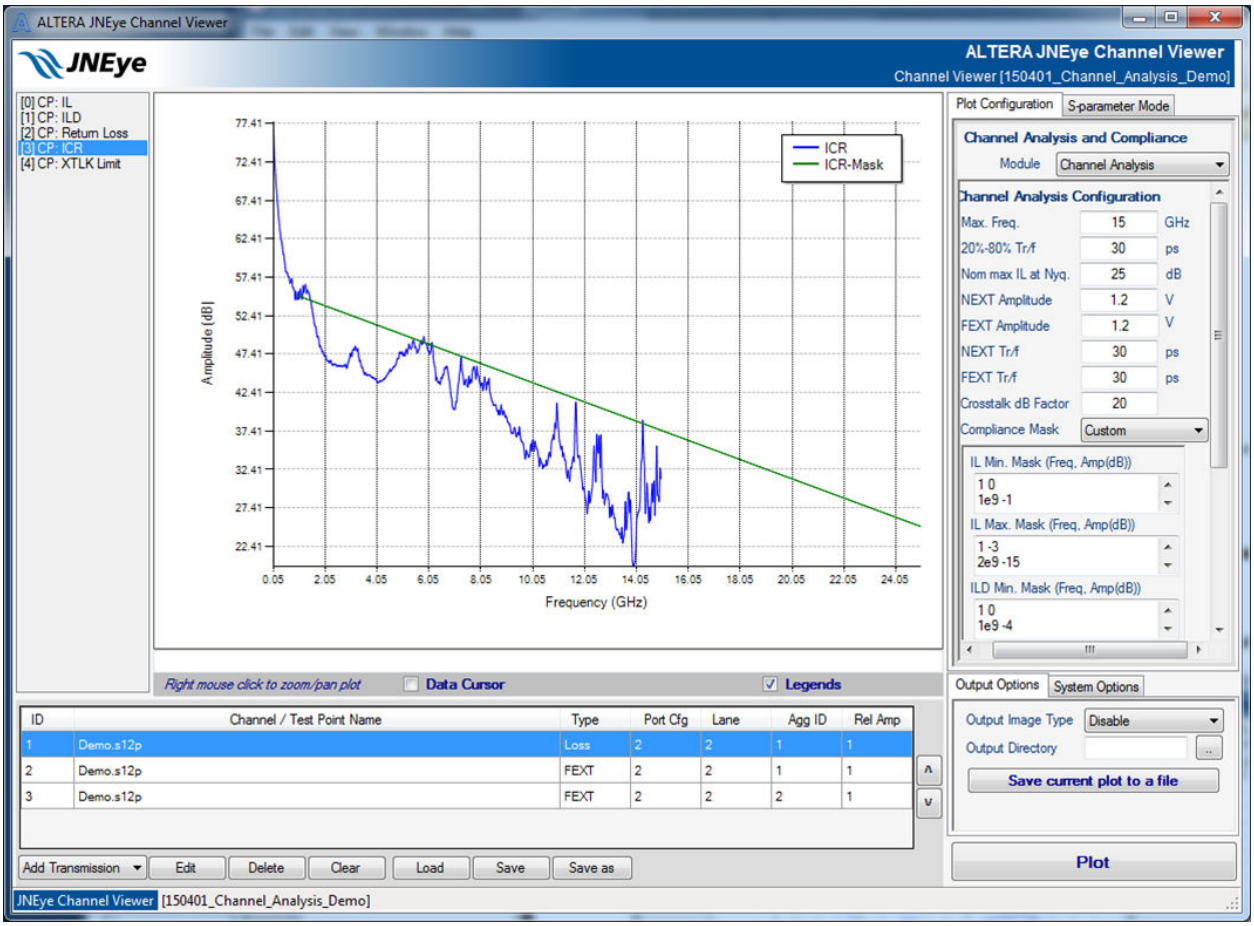
- **Return Loss** Plot—This plot is labeled **CP: RL**. In this plot, the return loss characteristics of channels are shown, as in the following figure.

Figure 2-95: Channel Analysis Module's Return Loss (RL) Analysis Example



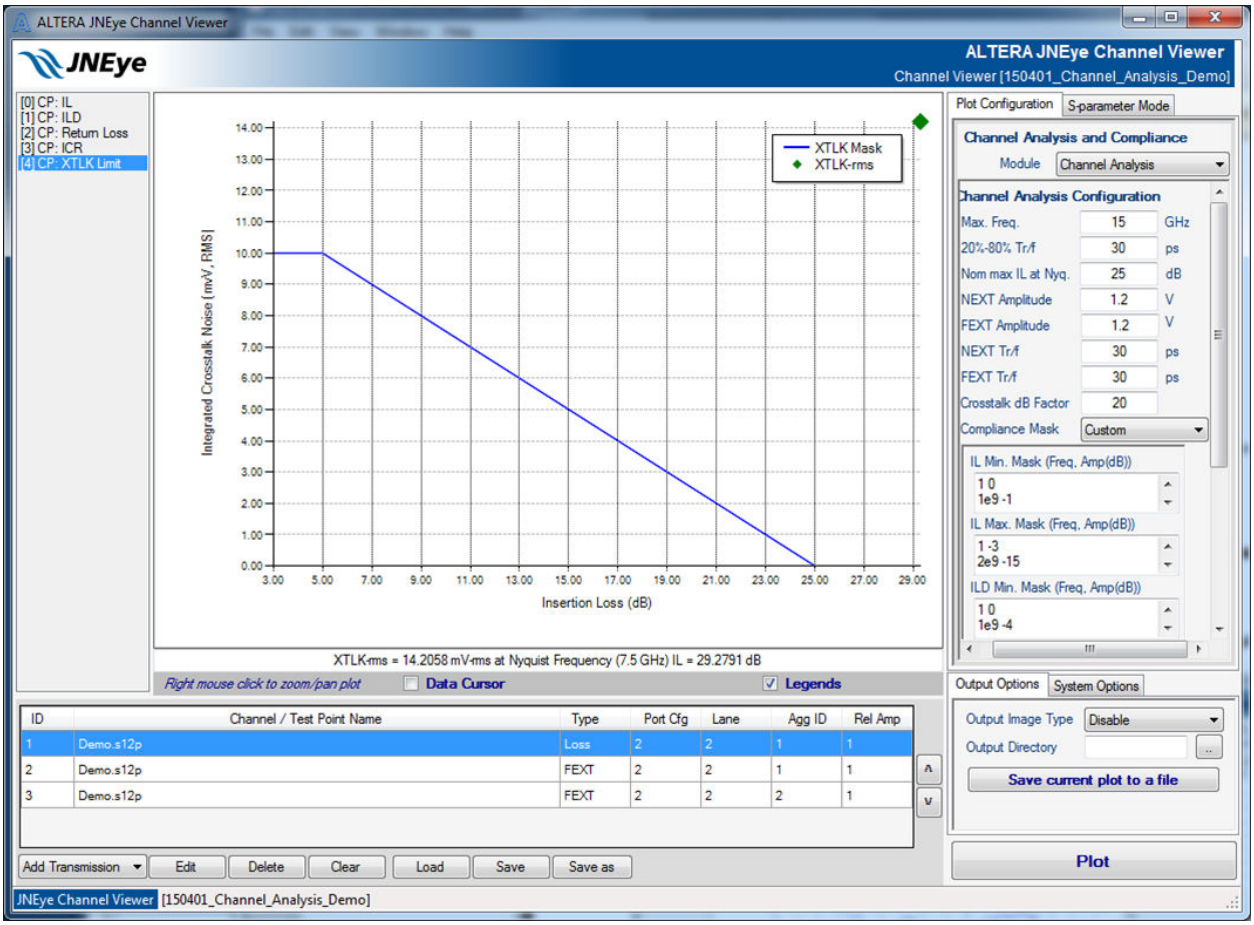
- **Insertion Loss to Crosstalk Ratio** Plot—This plot is labeled **CP: ICR**. In this plot, the Insertion Loss to Crosstalk Ratio (ICR) of channels is plotted. ICR is calculated as the distance between the insertion loss and combined crosstalk channels, as in the following figure.

Figure 2-96: Channel Analysis Module's Insertion Loss to Crosstalk Ratio (ICR) Analysis Example



- **Crosstalk Limit** Plot—This plot is labeled **CP: XTLK Limit**. In this plot, a crosstalk noise figure, XTLKrms in mV at Nyquist frequency, is calculated based on the user configurations, as in the following figure.

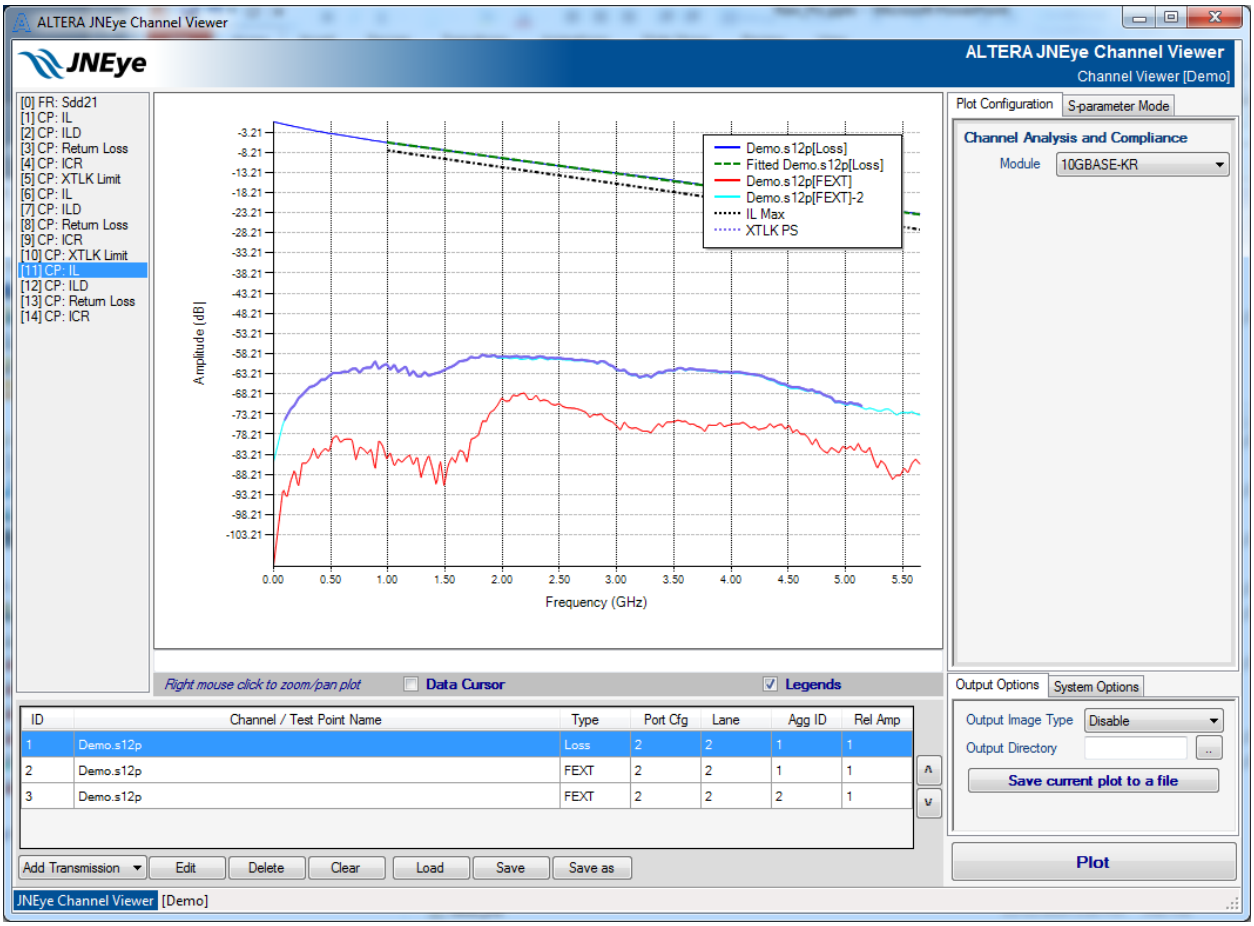
Figure 2-97: Channel Analysis Module's Crosstalk Limit Analysis Example



10GBASE-KR Channel Compliance

The following figure shows the 10GBASE-KR channel compliance check GUI.

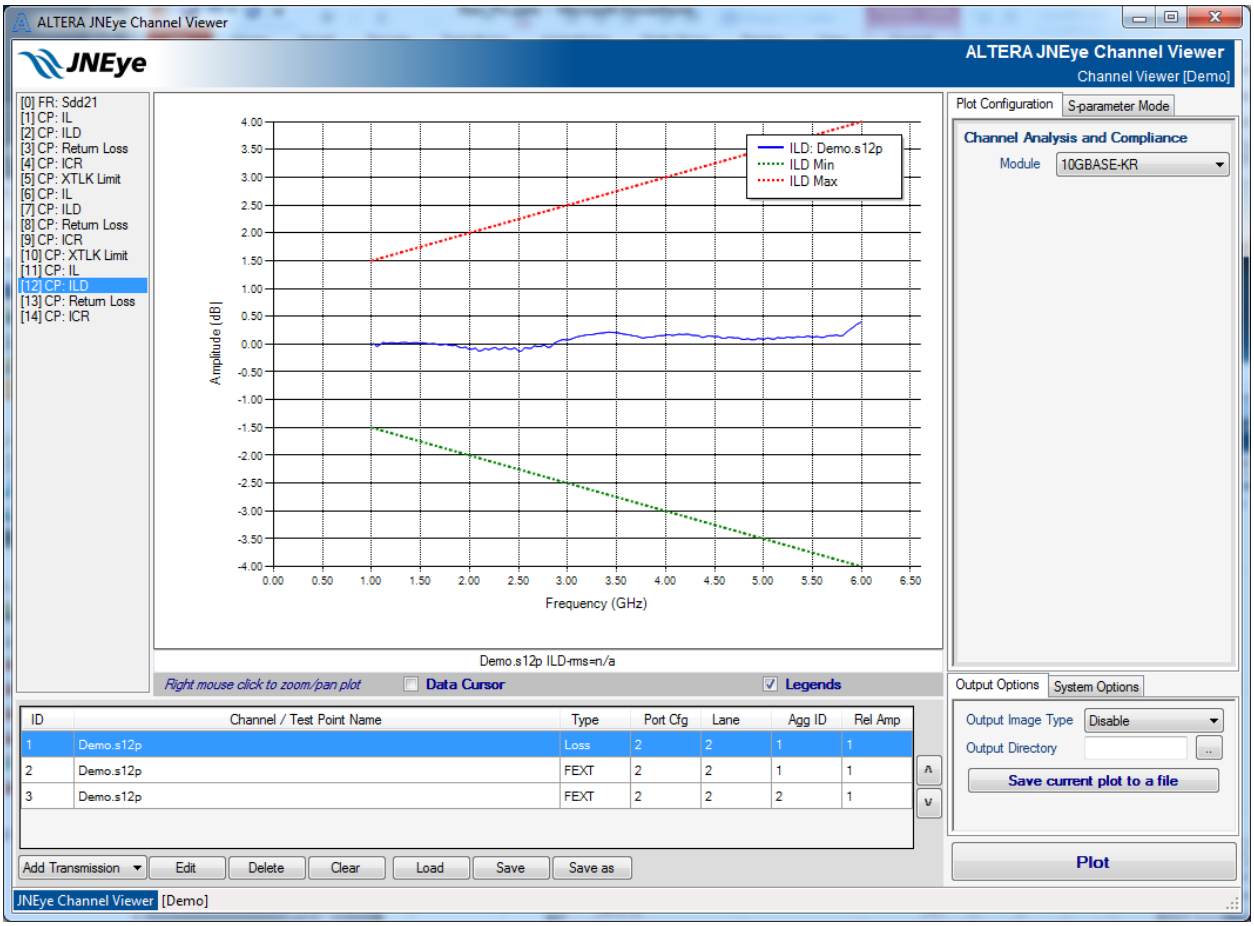
Figure 2-98: 10GBASE-KR Channel Compliance Check User Interface



All parameters are predefined as described in the IEEE 802.3ap/10GBASE-KR standards, so there is no user input. Click **Plot** to proceed. Channel Viewer computes and generates a sequence of plots that show the performance of the channels in the channel list.

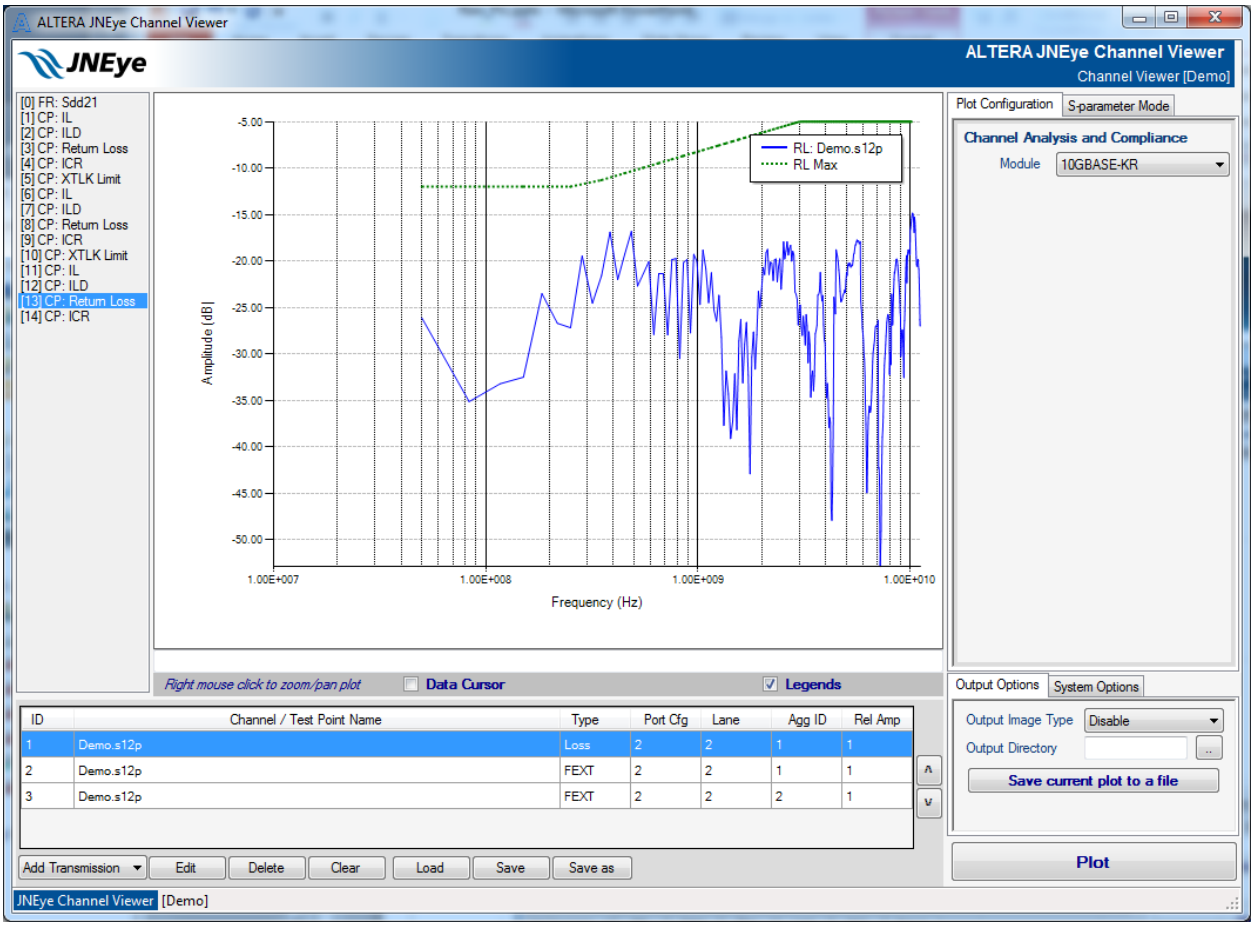
- **Insertion Loss** Plot—This plot is labeled **CP: IL**. In this plot, the insertion loss of channels, fitted curve of transmission channels' insertion loss, maximum insertion loss limits, crosstalk channels' amplitude, and power sum of all crosstalk channels is shown. An example is illustrated in the above figure.
- **Insertion Loss Deviation** Plot—This plot is labeled **CP: ILD**. In this plot, the insertion loss deviation and ILD masks are shown, as in the following figure.

Figure 2-99: 10GBASE-KR Channel Compliance Module's Insertion Loss Deviation (ILD) Analysis Example



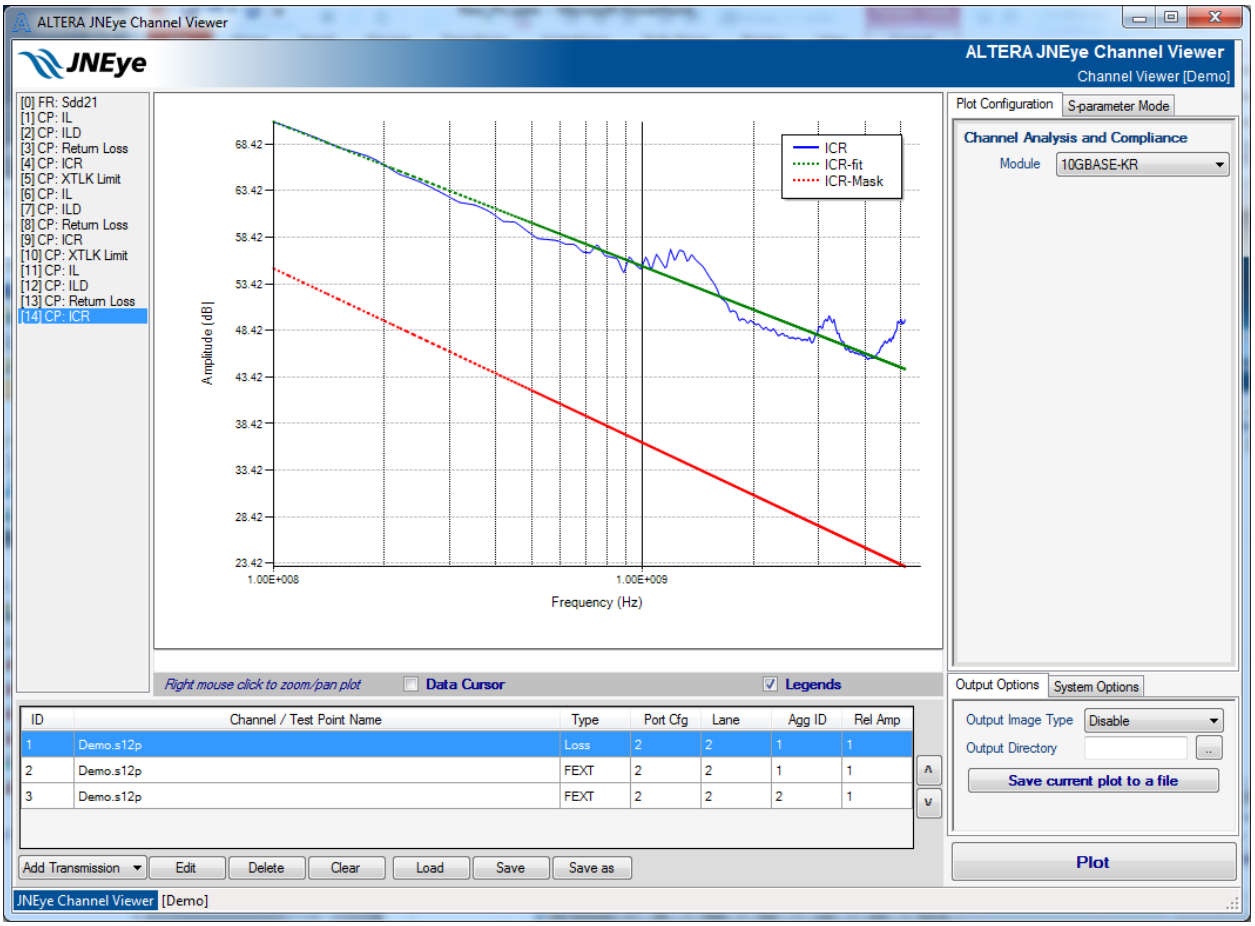
- **Return Loss** Plot—This plot is labeled **CP: RL**. In this plot, return loss (RL) characteristics of channels and the RL mask are shown, as in the following figure.

Figure 2-100: 10GBASE-KR Channel Compliance Module's Return Loss (RL) Analysis Example



- **Insertion Loss to Crosstalk Ratio** Plot—This plot is labeled **CP: ICR**. In this plot, the Insertion Loss to Crosstalk Ratio (ICR) of channels and the ICR mask are plotted, as in the following figure.

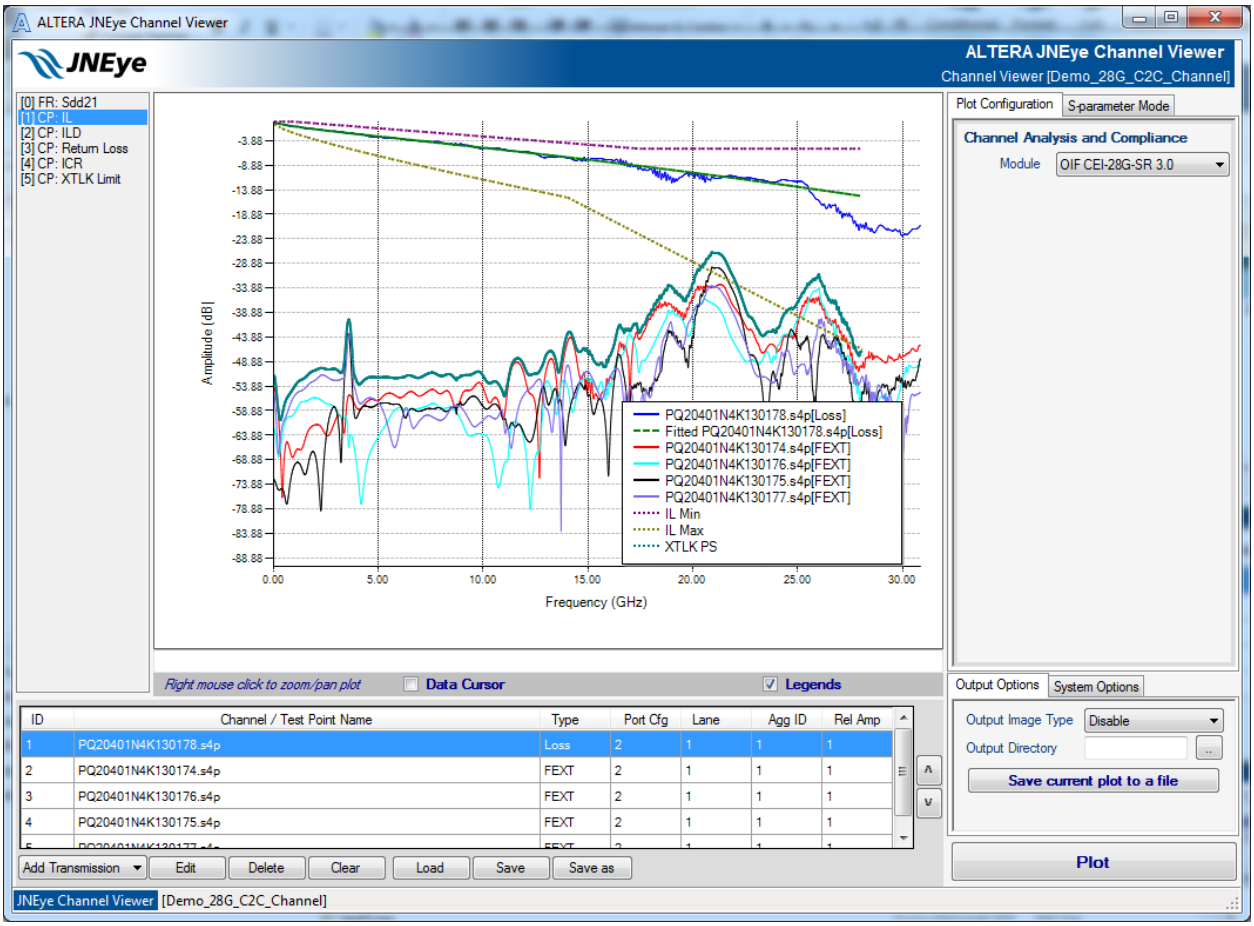
Figure 2-101: 10GBASE-KR Channel Compliance Module's Insertion Loss to Crosstalk Ratio (ICR) Analysis Example



OIF CEI-28G-SR 3.0 and OIF CEI-25G-LR Channel Compliances

The following figure shows the OIF CEI-28G-SR 3.0 channel compliance check GUI.

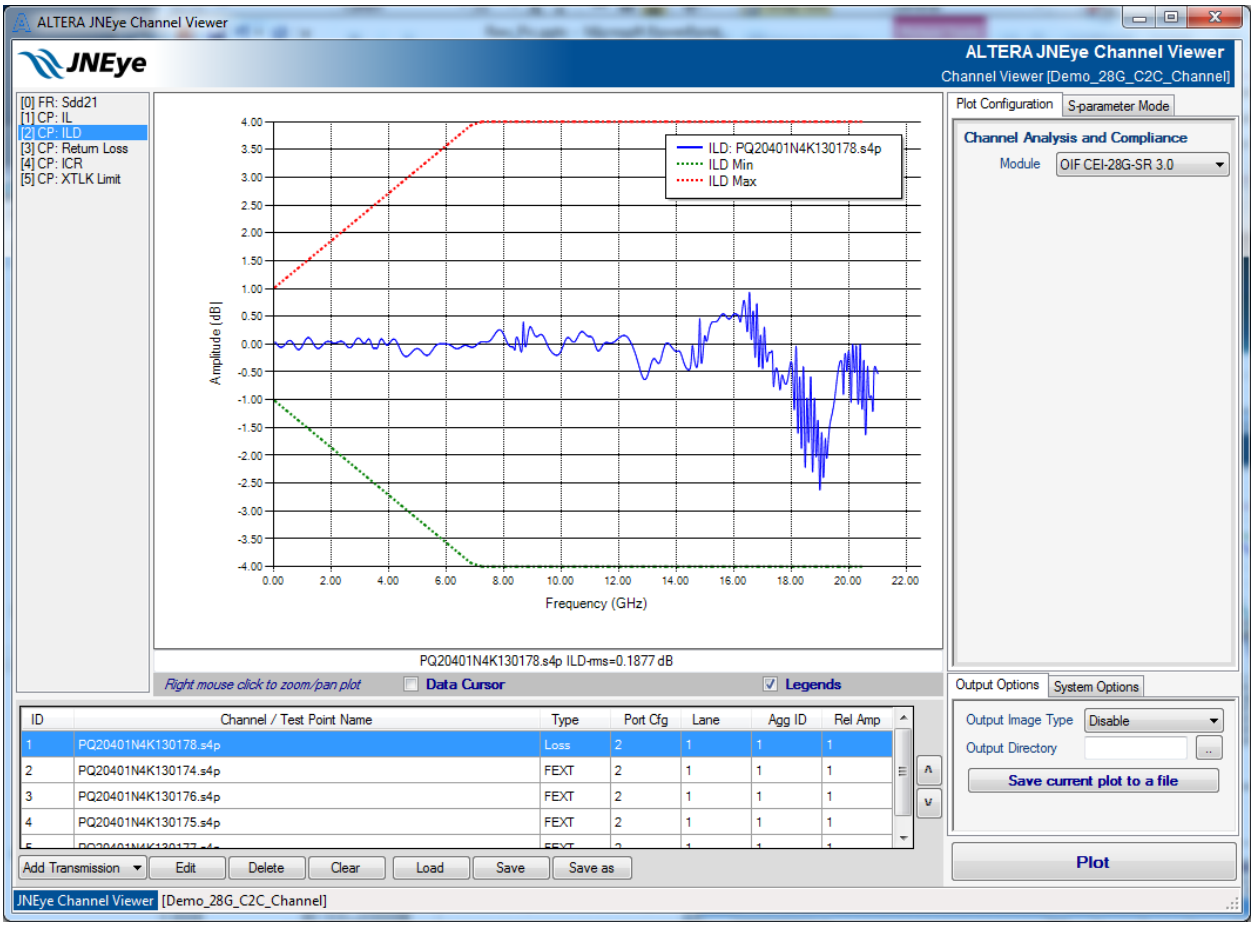
Figure 2-102: OIF CEI-28G-SR 3.0 Channel Compliance Check User Interface



OIF CEI-25G-LR, OIF CEI-28G-MR, and OIF-CEI-28G-SR channel compliances are similar in configuration and usage. Both cases are covered in this section. All parameters are predefined as described in the OIF CEI-25G-LR, OIF CEI-28G-MR, and OIF-CEI-28G-SR standards, so there is no user input. Click **Plot** to proceed. Channel Viewer computes and generates a sequence of plots that show the performance of the channels in the channel list.

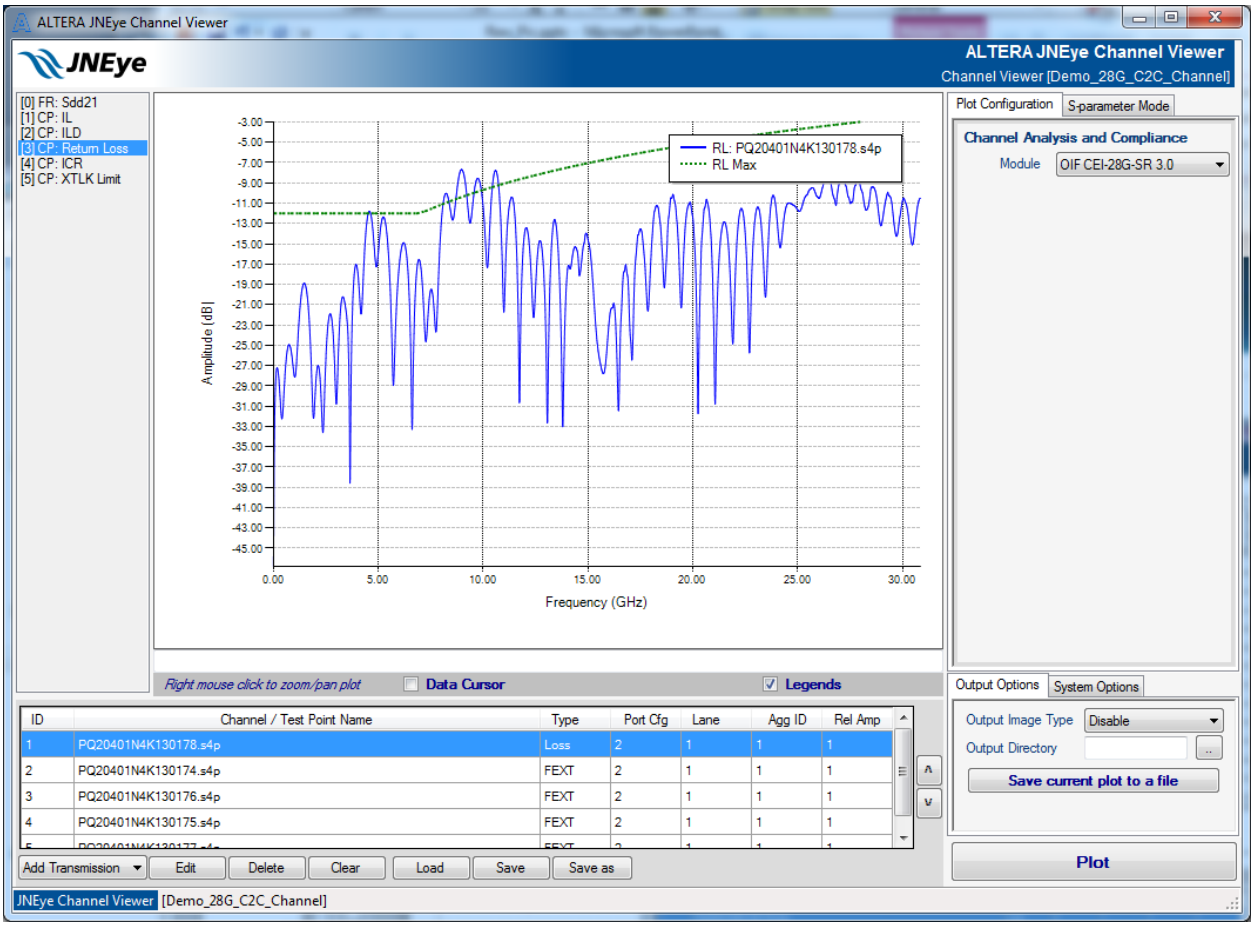
- **Insertion Loss** Plot—This plot is labeled **CP: IL**. In this plot, the insertion loss of channels, fitted curve of transmission channels' insertion loss, insertion loss masks, crosstalk channels' amplitude, and power sum of all crosstalk channels are shown. An example is illustrated in athe above figure.
- **Insertion Loss Deviation** Plot—This plot is labeled **CP: ILD**. In this plot, the insertion loss deviation and ILD masks are shown, as in the following figure.

Figure 2-103: OIF CEI-28G_SR 3.0 Channel Compliance Module's Insertion Loss Deviation (ILD) Analysis Example



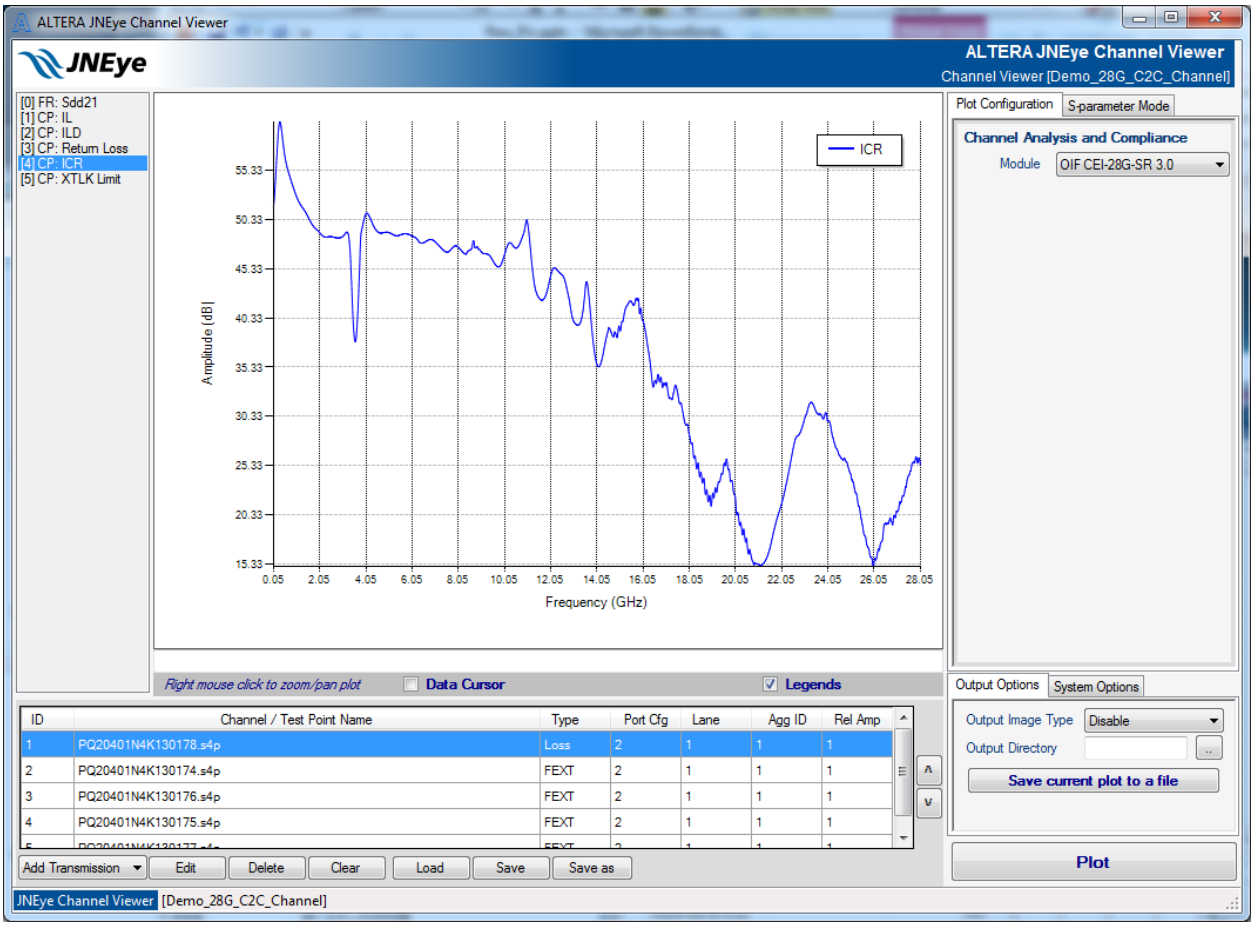
- **Return Loss** Plot—This plot is labeled **CP: RL**. In this plot, return loss (RL) characteristics of channels and RL mask are shown, as in the following figure.

Figure 2-104: OIF CEI-28G-SR 3.0 Channel Compliance Module's Return Loss (RL) Analysis Example



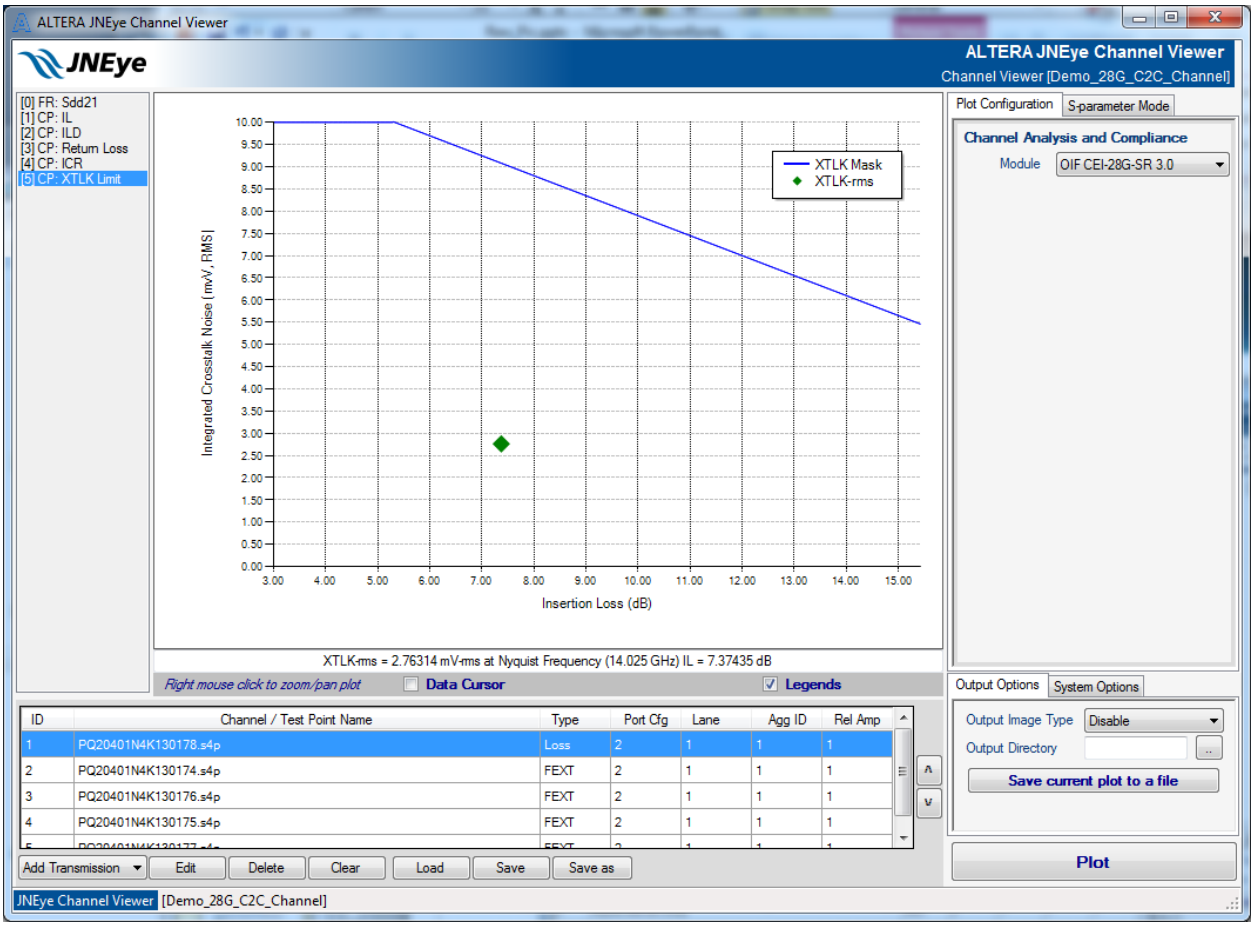
- **Insertion Loss to Crosstalk Ratio** Plot—This plot is labeled **CP: ICR**. In this plot, the Insertion Loss to Crosstalk Ratio (ICR) of channels and the ICR mask are plotted, as in the following figure.

Figure 2-105: OIF CEI-28G-SR 3.0 Channel Compliance Module's Insertion Loss to Crosstalk Ratio (ICR) Analysis Example



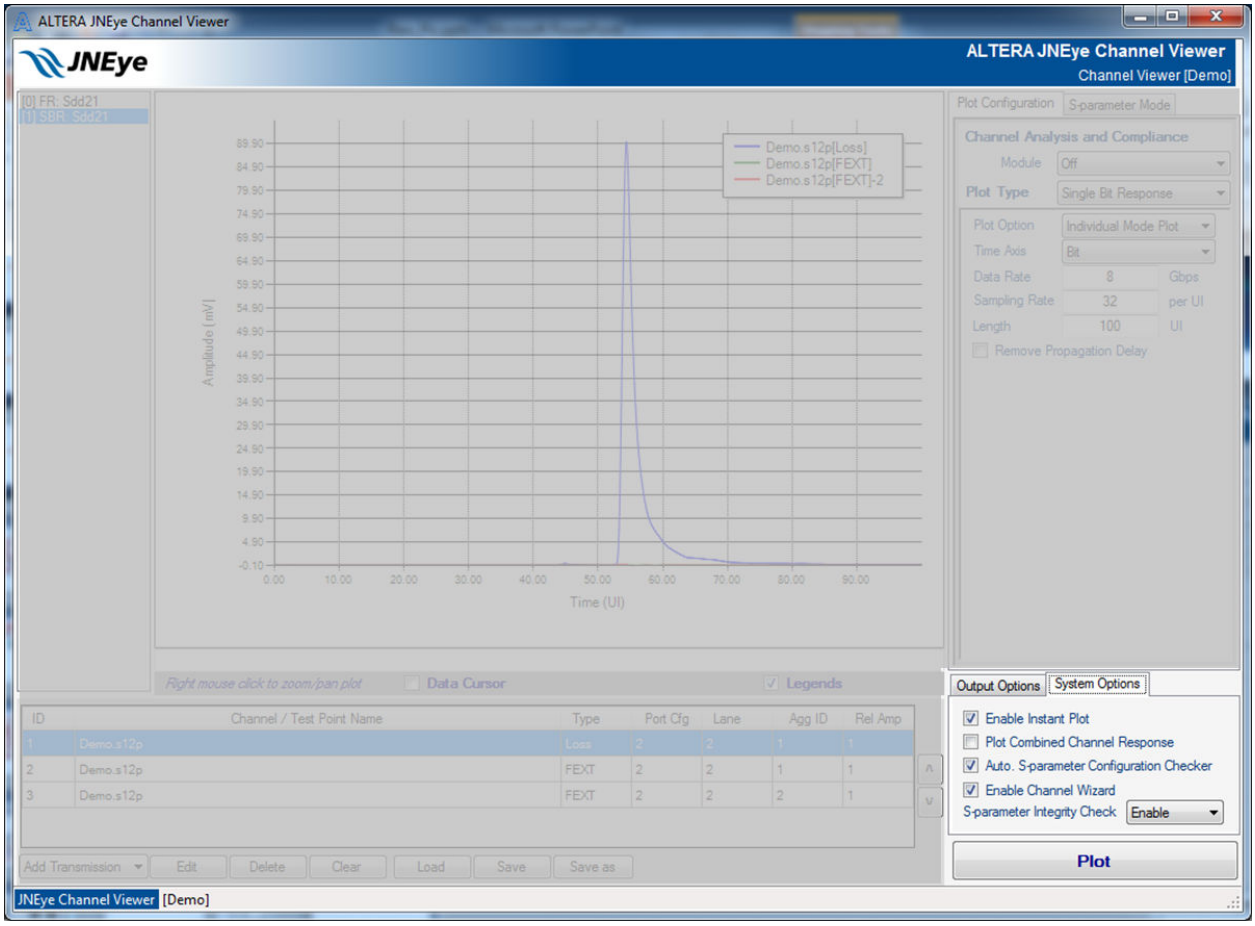
- **Crosstalk Limit** Plot—This plot is labeled **CP: XTLK Limit**. In this plot, a crosstalk noise figure, XTLKrms in mV at Nyquist frequency, is calculated based on the user configurations, as in the following figure

Figure 2-106: OIF CEI-28G-SR 3.0 Channel Analysis Module's Crosstalk Limit Analysis Example



Options Panel

Figure 2-107: Options Panel



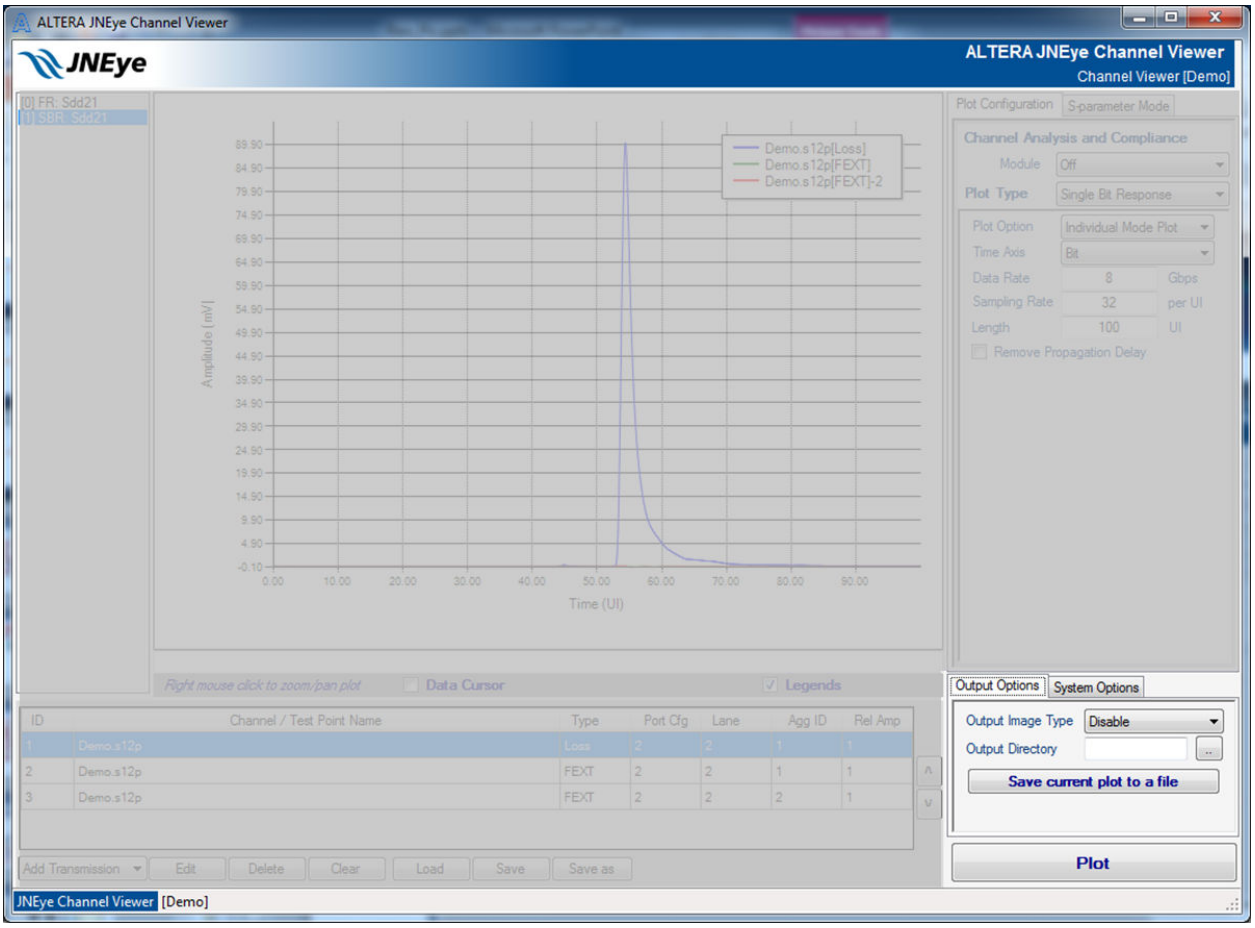
Use this panel to select the following plot options:

- **Enable Instant Plot**—Enable and disable instant channel plotting when a new channel is added to the channel list. When you disable this option, you must click **Plot** to plot the channel response.
- **Plot Combined Channel Response**—When you enable this option, the Channel Observer cascades the channels with Loss type and plots it along with other channel characteristics. The crosstalk channels (NEXT and FEXT) are not cascaded.
- **Auto. S-parameter Configuration Checker** (ASCC)—Enable and disable the ASCC function. The Channel Viewer uses the ASCC function to determine the port configuration of S-parameters. When you disable ASCC, you must manually select the port configuration of each S-parameter channel model.
- **Enable Channel Wizard**—If checked, when you select a channel file, Channel Wizard helps configure the channel configuration. If unchecked, you must manually configure the channel configuration.
- **S-parameter Integrity Check**—If enabled, Channel Wizard checks the channel integrity (the passivity and causality). If JNEye has problems with opening or accessing an S-parameter, you can disable the S-parameter Integrity Check.

Output Options Panel

To generate images of new channel plots, click **Save current plot to a file** when the Output Image Type menu is set to **PNG**, **JPG**, or **GIF**. A file browser opens to help you find a location for the image file. You can also specify an output directory where the output image files are saved when **Output Image File** is set.

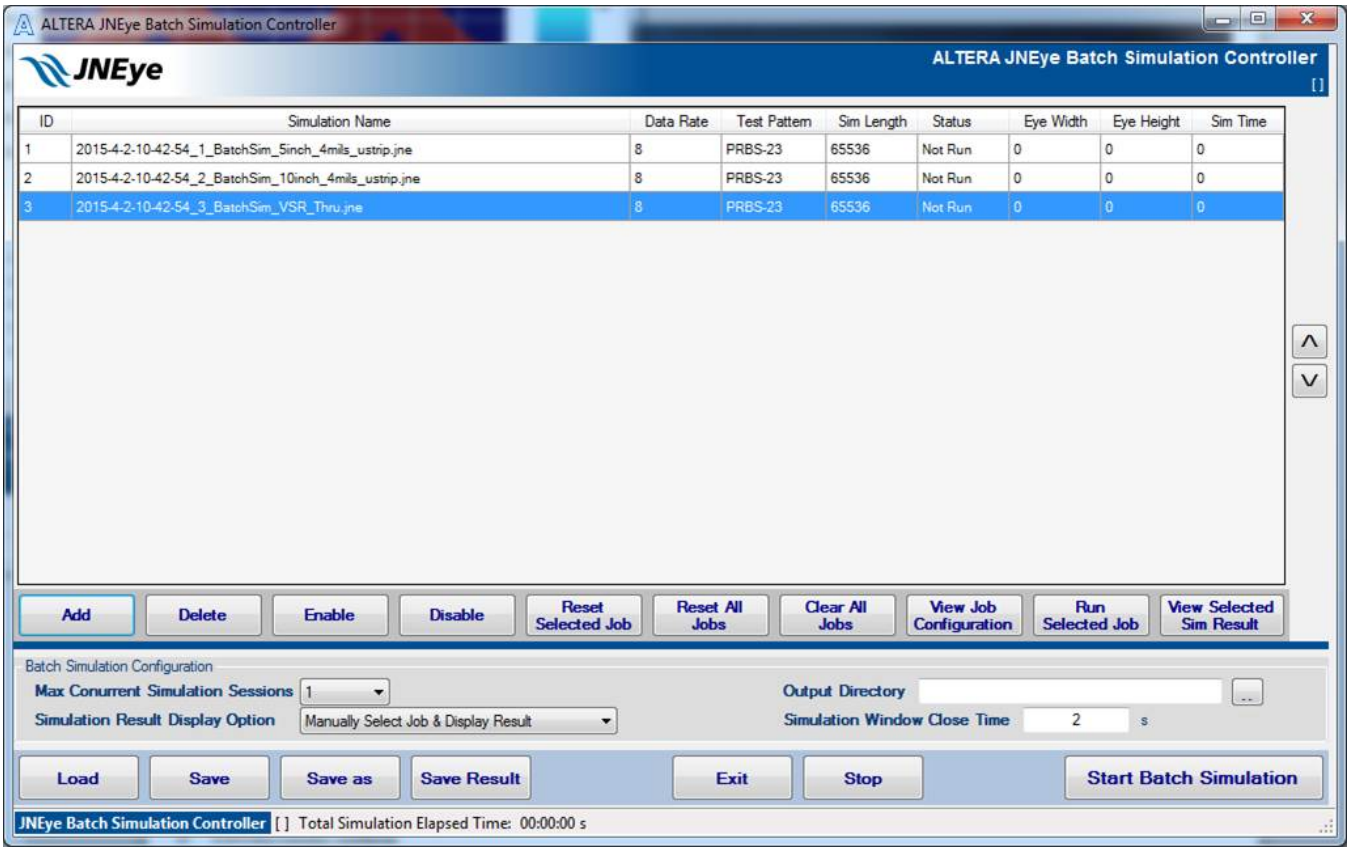
Figure 2-108: Output Options Panel



JNEye Batch Simulation Controller

The JNEye Batch Simulation Controller allows you to run multiple simulations by not invoking the JNEye Control Module. This capability allows you to run multiple link simulations and then review the results offline.

Figure 2-109: JNEye Batch Simulation Controller



The JNEye Batch Simulation Controller accepts JNEye simulation configuration (**.jne**) files. You can set up and save their link simulation configurations using JNEye Control Module. You can then add each individual JNEye job to the batch job list and execute all the jobs.

The JNEye Batch Simulation Controller has a built-in timer and house-keeping routine that constantly monitors the status of simulating tasks. It can also launch more than one simulation job at a time to better utilize the multi-core/multi-processor computing environment. Check whether your JNEye license or license server supports multiple simulations at the same time.

After adding jobs, some key job information is shown in the job list, including simulation data rate, test pattern, simulation length, and initial job status of "Not Run". After simulation, key simulation results, such as the final eye diagram height and weight, are displayed in the job list along with the simulation time.

The following options are available in the JNEye Batch Simulation Controller user interface:

- **Add**—Add a JNEye simulation job to the job list. Use the file browser to locate **.jne** configuration files.
- **Delete**—Delete the highlighted job in the job list.
- **Enable/Disable**—Enable or disable the highlighted job in the job list.
- **Reset Select Jobs**—Reset the status of highlighted jobs to "Not Run"
- **Reset All Jobs**—Reset all jobs in the job list to "Not Run"
- **Clear All Jobs**—Clear and delete all jobs in the job list
- **View Job Configuration**—Open and load JNEye Control Module with the highlighted job
- **Run Selected Job**—Execute the highlighted job

- **View Select Sim Result**—Open and load simulation result (if available) of the selected job
- **Move Up** (/\)—Move the highlighted job forward in the job list
- **Move Down** (\/)—Move the highlighted job toward to back of the job list
- **Load**— Load JNEye Batch Simulation Controller configuration file
- **Save/Save as**—Save or save new JNEye Batch Simulation Controller configuration file
- **Exit**—Exit the JNEye Batch Simulation Controller
- **Stop**—Stop batch simulation of jobs
- **Start Batch Simulation**—Start batch simulation of all not-executed jobs in the job list
- **Maximum Concurrent Simulation Session**—Set the number of concurrent simulations. JNEye Batch Simulation Controller monitors the number of executing jobs. It starts a new simulation job when the computing resource is available.
- **Simulation Result Display Option**—This menu controls the simulation result display option. There are three options:
  - **Display Result**—When each simulation is completed, a new Data Viewer window will open and show the result.
  - **Ask to Display Result**—When each simulation is completed, a message box will open and ask if the simulation results will be shown.
  - **Manually Select Job & Display Result**—This is the default option. When a job is finished, no result will be shown. You must manually select the job and click **View Selected Sim Result** to see the simulation results.
- **Simulation Window Close Time**—When a simulation is completed, the JNEye Simulation Engine window will remain open for the specified time before closing.
- **Output Directory**—Specify the output directory where all the batch simulation results will be saved. This output location overrides the output directory option specified in each individual simulation job.

Notes:

- JNEye Batch Simulation Controller launches each job in an individual process. Make sure there are no file read/write access conflicts. The most common issue is that several jobs might want to open and/or modify the same file (for example, log file from IBIS-AMI models). This will cause the job process to fail.
- When a job fails to complete, it may occupy one simulation resource, such as the CPU, indefinitely. If this occurs, manually close the failing simulation engine to free the computing resource.
- Check your JNEye license type or license server configuration to see if simultaneous multiple simulations are supported. Some license servers do not allow you to check out multiple license at the same time.
- Altera recommends you run batch simulation with two or more concurrent sessions, if supported by the computation environment. This avoids blocking the batch simulation queue.
- Altera recommends you run batch simulations with the **Manual Select Job & Display Result** option because viewing all simulation results may take a large amount of computing resources.

JNEye Channel Designer

The JNEye Channel Designer (JCDE) allows you to design your own channel models.

JNEye Channel Designer (JCDE) contains the following channel components:

- Stripline
- Microstrip
- Coax
- RLGC transmission line

- Ideal transmission line
- Via model based on composite transmission line blocks
- Shunt and series capacitance
- Series inductance
- S-parameter model

A channel design can include one or multiple channel components. JNEye Channel Designer can combine and generate Touchstone S-parameter models that can be used in link simulations. JNEye Channel Designer provides user friendly and integrated interfaces. The channel components and resulting channel models can be observed and analyzed using embedded plot functions or the JNEye Channel Viewer.

In the 15.0 JNEye release, a 2-port single-ended channel model will be generated internally for all of the above components except the S-parameter model.

After the single-ended model is generated, JNEye Channel Designer converts it into a 4-port differential-pair format by assuming that these two single-ended channels are uncoupled. Channel cascading of all channel components, which include S-parameter channel components, are done in the 4-port level.

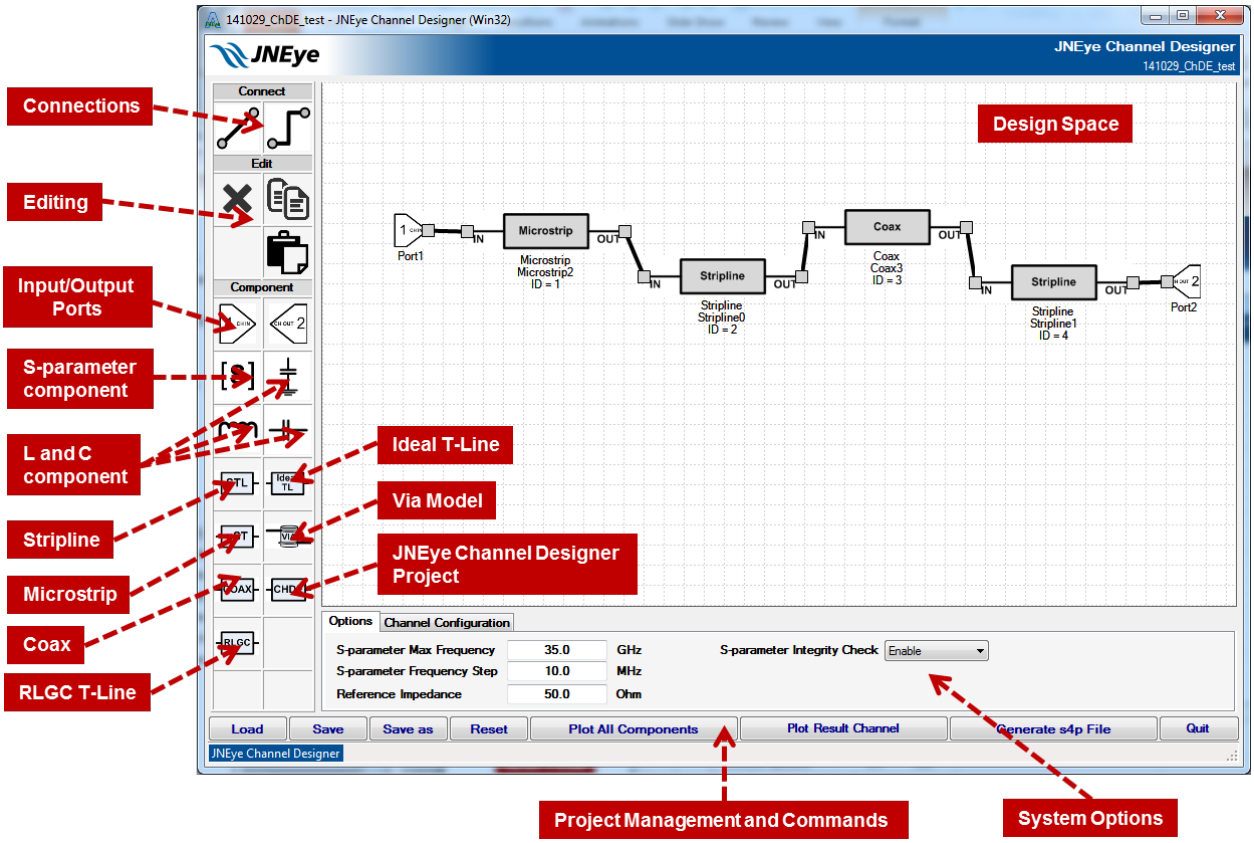
Starting the JNEye Channel Designer

You can start JNEye Channel Designer in two ways:

- Double-click **JNEye_Channel_Designer.exe**
- Click **Channel Designer** in the JNEye Control Module

The JNEye Channel Designer's graphical user interface is shown in the following figure.

Figure 2-110: JNEye Channel Designer User Interface



- **Connect**—Use the straight line or right-angled line to connect channel components
- **Edit**—User can use these commands to delete, copy, or paste channel components
- **Component**—Individual channel components to be added to the channel. See sessions below for details
- **Design Space**
- **System Options**—Set up system level parameters and options
  - **S-parameter Max Frequency**—Set the maximum frequency of the resulting channel model
  - **S-parameter Frequency Step**—Set the frequency step of the resulting channel model
  - **Reference Impedance**—Set the reference impedance of the resulting channel model
  - **S-parameter Integrity Check**—Select if channel integrity check, e.g. passivity and causality, will be performed on the input S-parameter model. If JNEye Channel Designer has issues opening or accessing certain S-parameter files, a user can disable the channel integrity check to see if the issue is resolved
- **Project management and Commands**
  - **Load**—Load previously saved Channel Designer project
  - **Save/Save as**—Save current project
  - **Reset**—Clear all channel components
  - **Plot All Components**—Plot all individual channel components in the Design Space using JNEye Channel Viewer
  - **Plot Result Channel**—Generate the result channel and plot its characteristics using JNEye Channel Viewer
  - **Generate s4p File**—Generate the result channel and save it in a 4-port Touchstone S-parameter file
  - **Quit**—Exit JNEye Channel Designer

Constructing a Channel in Channel Designer

Similar to the Link Designer operations in JNEye's Control Module, a channel consists of one or more channel components between the input port (Port 1) and the output port (Port 2). After the channel components are placed into the workspace, click **Connect** to connect the components. In Connect mode, one or two connectors are shown on each component. Connect the channel components by dragging the line from one connector to another. Two types of connections are provided in Channel Designer: **Right Angled Line** and **Straight Line**.

The following rules of channel construction apply to the Channel Designer:

- The Input port (Port 1) has one output port or connector
- The Output port (Port 2) has one input port or connector
- A channel component has one input and one output port
- A connection between two components can be established from an output port to an input port
- An input port cannot be connected directly to an output port

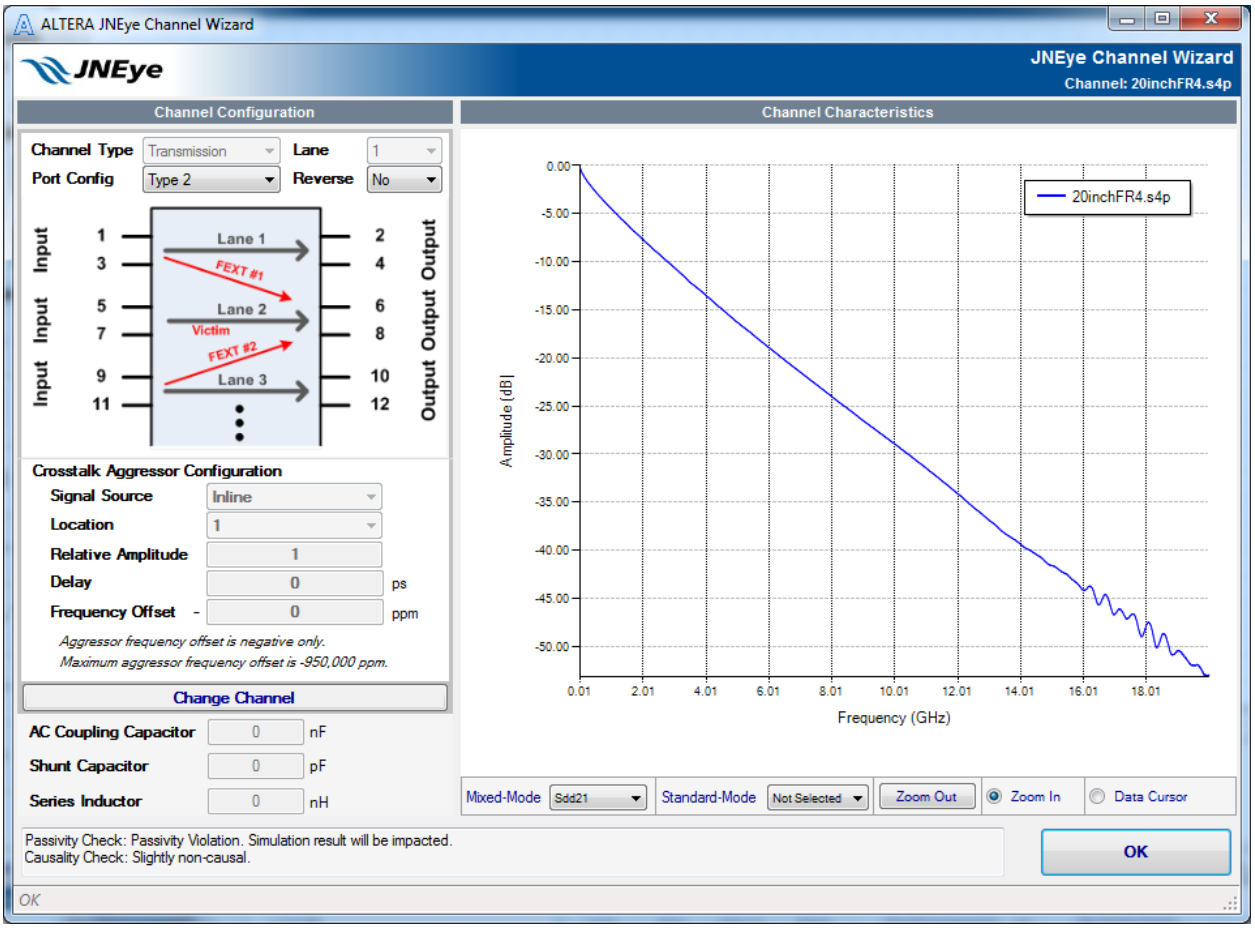
A channel establishment checking algorithm runs constantly in the background, checking whether a channel is established for channel generation. When a channel is established between an input port and an output port, the link lines become bold. The User Interface figure above shows an established channel link.

Channel Components

The Channel Designer contains the following components:

- **Port 1**—Port 1 is the input port of the channel under construction.
- **Port 2**—Port 2 is the output port of the channel under construction.
- **S-parameter channel component**—Use an S-parameter channel model file as part of the channel under construction. When you click the S-parameter icon, the Channel Wizard appears to help you configure the S-parameter file. Refer to the JNEye Control Module's Channel Wizard section for detailed usage. The following figure shows an example of the Channel Wizard.

Figure 2-111: Channel Wizard Example



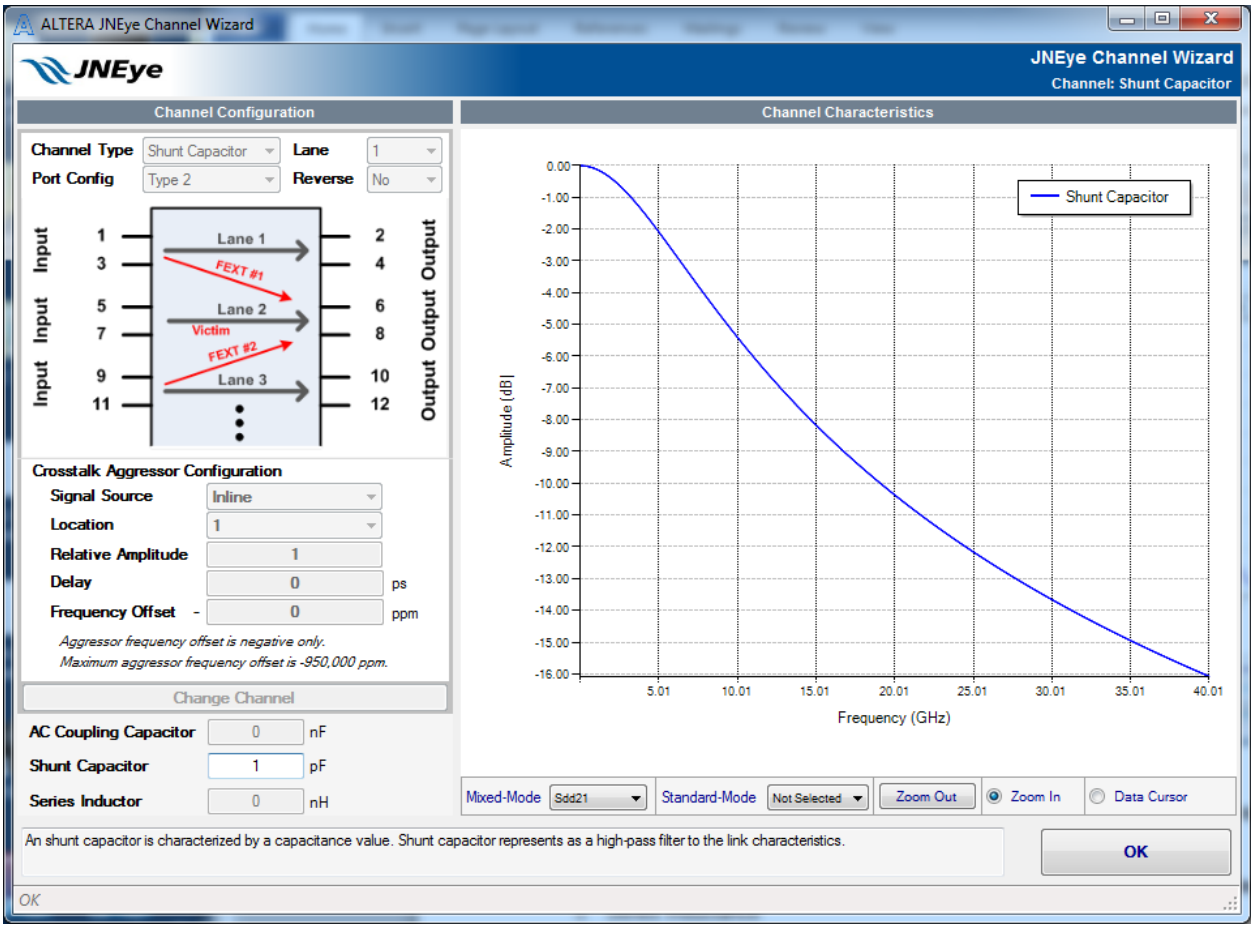
Capacitance and Inductance Model Components

You can insert the following capacitance and/or inductance components as part of the channel:

- **Shunt capacitance**
- **Series capacitance**—Listed in the Channel Wizard under the **AC Coupling Capacitor**
- **Series Inductance**

JNEye Channel Designer uses the Channel Wizard to configure these capacitance and inductance components so you can input the capacitance and inductance values there. The following figure shows an example.

Figure 2-112: Capacitance and Inductance Channel Component Configuration in Channel Wizard



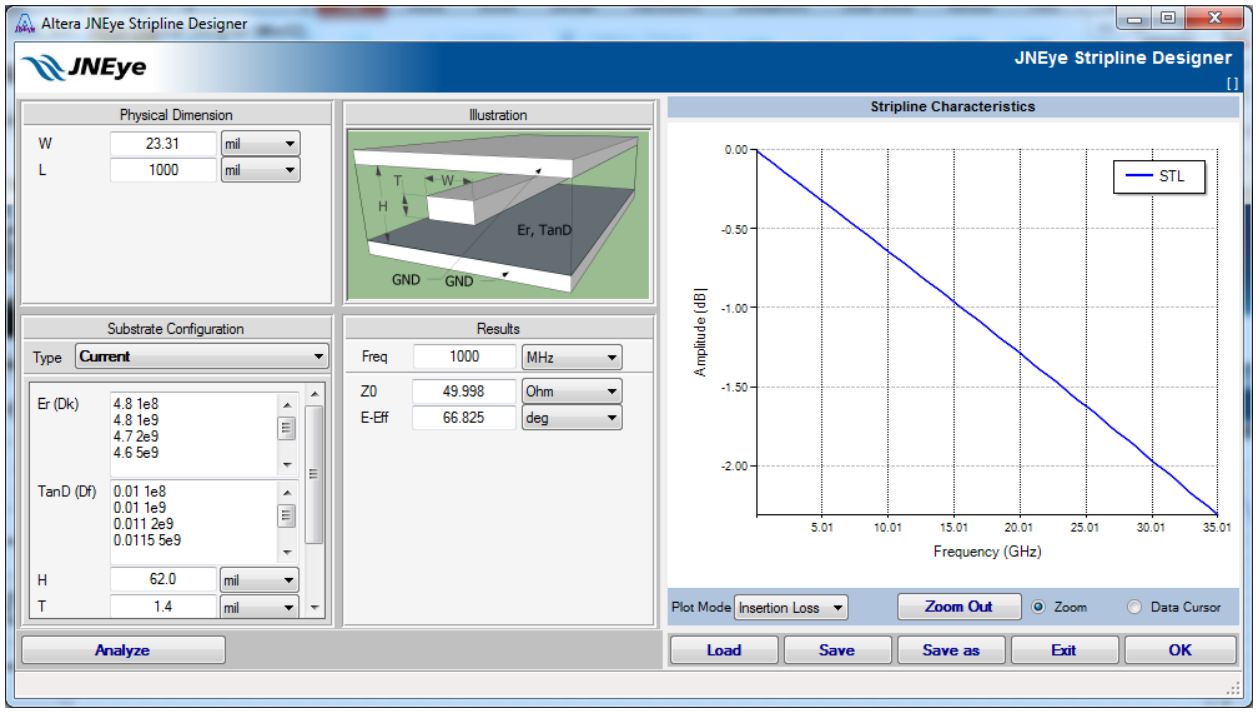
Stripline Component

A stripline uses a flat strip of metal that is sandwiched between two parallel ground planes. The insulating material of the substrate forms a dielectric. The width of the strip, the thickness of the substrate, and the

relative permittivity of the substrate determine the characteristic impedance of the strip which is a transmission line. A typical stripline structure is shown in the following figure with these parameters:

- Input parameters
  - **W**—Signal trace width (in various units)
  - **L**—Signal trace length (in various units)
  - **T**—Signal trace thickness (in various units)
  - **H**—Separation between ground planes (in various units)
  - **Er (Dk)**—Relative dielectric constant. JNEye Channel Designer supports frequency dependent dielectric constant mapping.
  - **TanD (Df)**—Dielectric loss tangent. JNEye Channel Designer supports frequency dependent dissipation factor mapping.
  - **Cond**—Conductor conductivity (S/m)
  - **Rough**—Surface roughness (in various units)
  - **Mur**—Relative permeability (no unit)
  - **Freq**—Frequency where the Z0 (Impedance) and E-Eff (electrical length) are reported (in various units)
- Output parameters
  - **Z0**—Impedance at specified frequency **Freq** (Ohm)
  - **E-Eff**—Electrical length (in various units)

Figure 2-113: Stripline Channel Component Configuration



The channel component designer GUI can perform parameter unit conversion interactively. For example, you can change the length unit from mil to mm and the GUI will automatically compute the length value with the new unit.

After entering the model parameters, click **Analyze** and Channel Designer will compute the frequency response of the current design. The integrated plotting engine can display the **insertion loss** or **return loss** characteristics. When you alter the model parameters, the GUI displays a message that indicates the channel characteristics may have changed. Click **Analyze** to redraw the channel characteristics. You can also **load** or **save** the component design for reuse in the future.

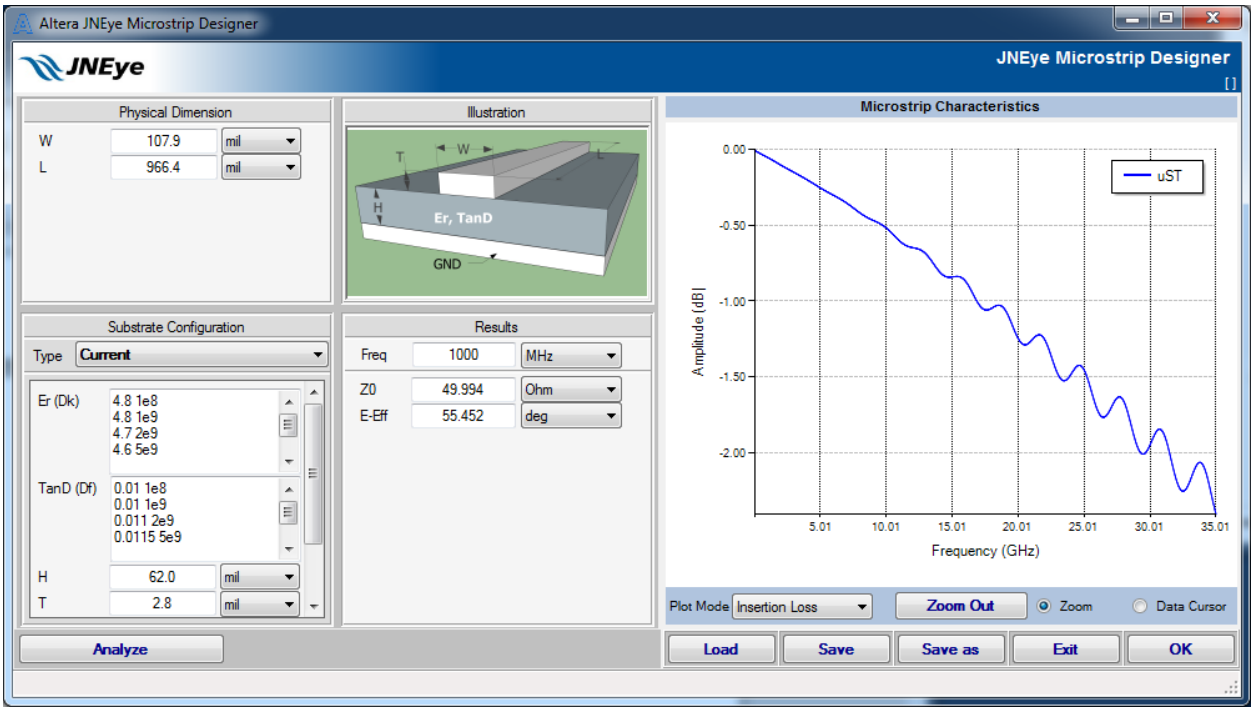
If you are satisfied with your design, click **OK** to save and close the component design GUI. If you click **Exit** or the **X** button of the window, the design will be discarded.

Microstrip Component

Microstrip is a type of electrical transmission line. It consists of a conducting strip separated from a ground plane by a dielectric layer known as the substrate. A typical microstrip structure is shown in the following figure with these parameters:

- Input parameters
  - **W**—Signal trace width (in various units)
  - **L**—Signal trace length (in various units)
  - **T**—Signal trace thickness (in various units)
  - **H**—Separation between ground planes (in various units)
  - **Er (Dk)**—Relative dielectric constant. JNEye Channel Designer supports frequency dependent dielectric constant mapping.
  - **TanD (Df)**—Dielectric loss tangent. JNEye Channel Designer supports frequency dependent dissipation factor mapping.
  - **Cond**—Conductor conductivity (S/m)
  - **Rough**—Surface roughness (in various units)
  - **Mur**—Relative permeability (no unit)
  - **Freq**—Frequency where the Z0 (Impedance) and E-Eff (electrical length) are reported (in various units)
- Output parameters
  - **Z0**—Impedance at specified frequency **Freq** (Ohm)
  - **E-Eff**—Electrical length (in various units)

Figure 2-114: Microstrip Channel Component Configuration



The channel component designer GUI can perform parameter unit conversion interactively. For example, you can change the length unit from mil to mm and the GUI will automatically compute the length value with the new unit.

After entering the model parameters, click **Analyze** and Channel Designer will compute the frequency response of the current design. The integrated plotting engine can display the **insertion loss** or **return loss** characteristics. When you alter the model parameters, the GUI displays a message that indicates the channel characteristics may have changed. Click **Analyze** to redraw the channel characteristics. You can also **load** or **save** the component design for reuse in the future.

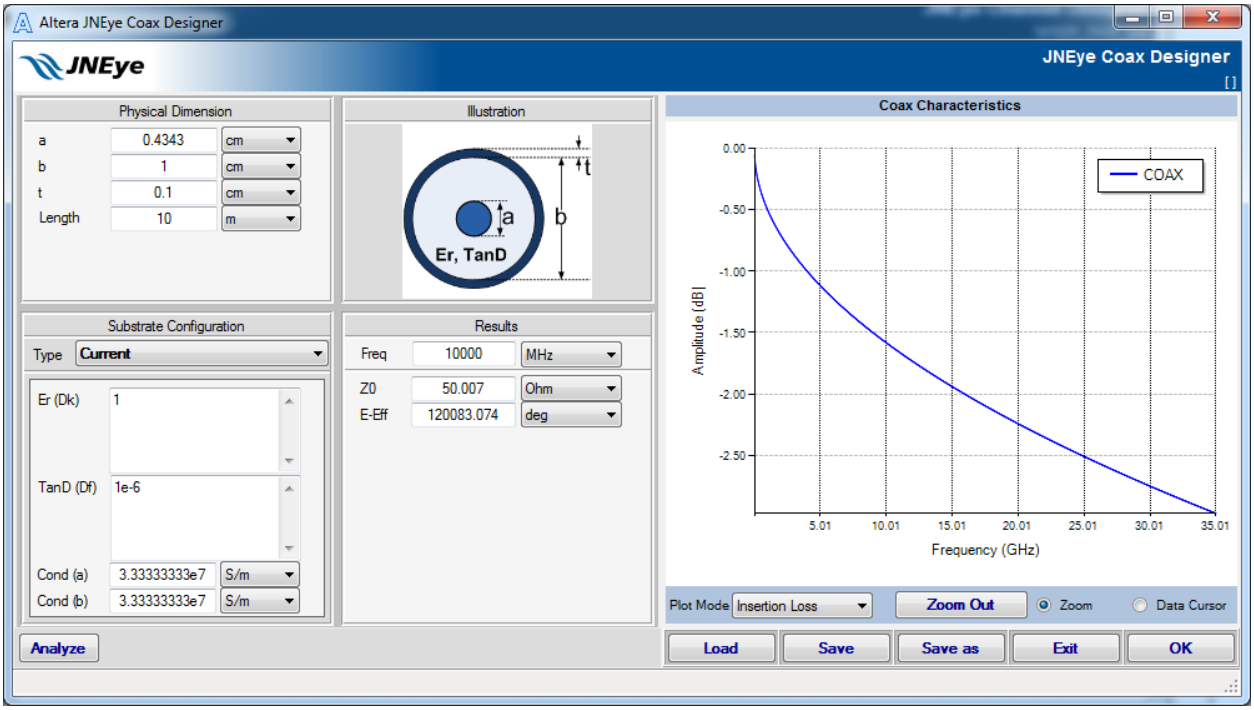
If you are satisfied with your design, click **OK** to save and close the component design GUI. If you click **Exit** or the **X** button of the window, the design will be discarded.

Coax Component

A coax transmission line consists of two round conductors in which one completely surrounds the other. The two conductors are separated by a continuous solid dielectric. A typical coax structure is shown in the following figure with these parameters:

- Input parameters
  - **a**—Diameter of inner conductor (in various units)
  - **b**—Diameter of outer conductor (in various units)
  - **t**—Thickness of outer conductor (in various units)
  - **Length**—Length of the coax (in various units)
  - **Er (Dk)**—Relative dielectric constant. JNEye Channel Designer supports frequency dependent dielectric constant mapping.
  - **TanD (Df)**—Dielectric loss tangent. JNEye Channel Designer supports frequency dependent dissipation factor mapping.
  - **Cond (a)**—Conductor conductivity of inner conductor (S/m)
  - **Cond (b)**—Conductor conductivity of outer conductor (S/m)
  - **Freq**—Frequency where the Z0 (Impedance) and E-Eff (electrical length) are reported (in various units)
- Output parameters
  - **Z0**—Impedance at specified frequency **Freq** (Ohm)
  - **E-Eff**—Electrical length (in various units)

Figure 2-115: Coax Channel Component Configuration



The channel component designer GUI can perform parameter unit conversion interactively. For example, you can change the length unit from mil to mm and the GUI will automatically compute the length value with the new unit.

After entering the model parameters, click **Analyze** and Channel Designer will compute the frequency response of the current design. The integrated plotting engine can display the **insertion loss** or **return loss** characteristics. When you alter the model parameters, the GUI displays a message that indicates the channel characteristics may have changed. Click **Analyze** to redraw the channel characteristics. You can also **load** or **save** the component design for reuse in the future.

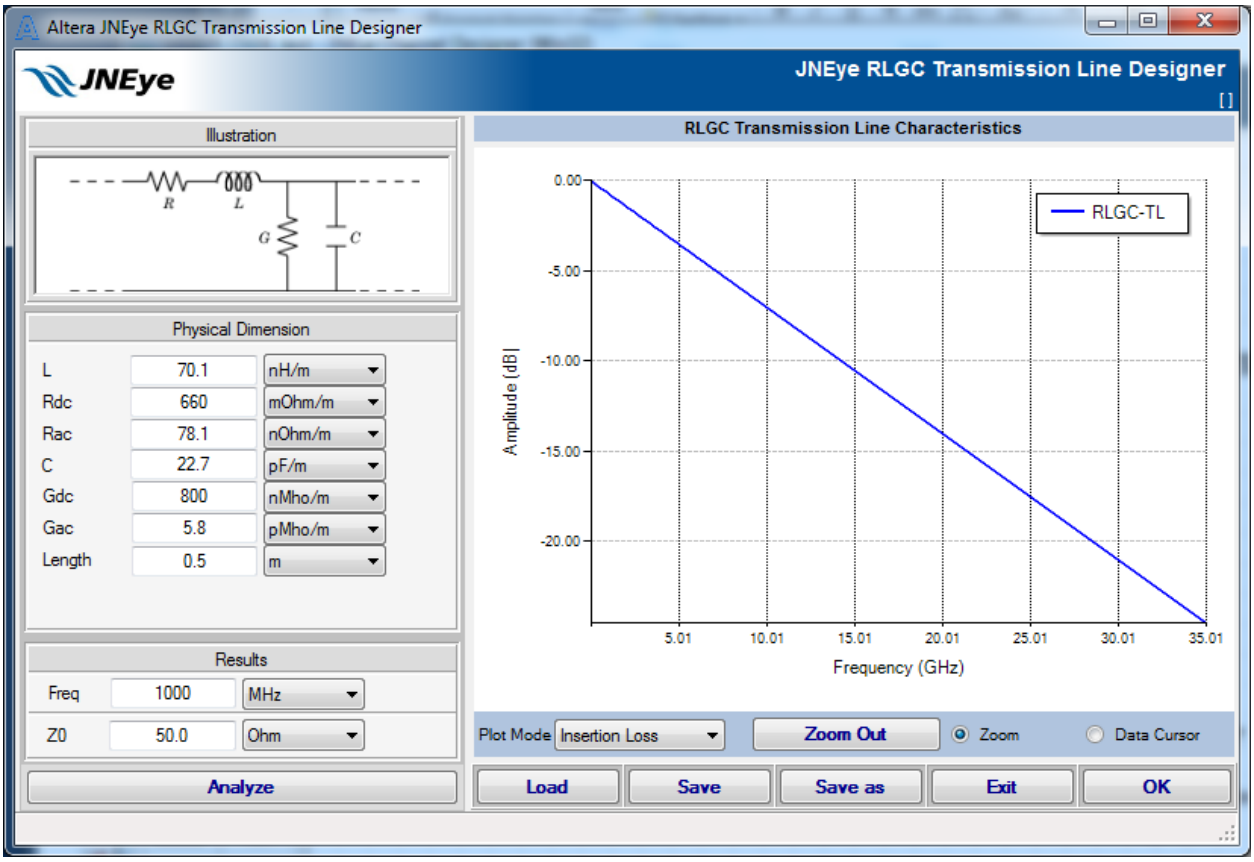
If you are satisfied with your design, click **OK** to save and close the component design GUI. If you click **Exit** or the **X** button of the window, the design will be discarded.

RLGC Transmission Line Component

The channel will be constructed with unit length RLGC models. A typical RLGC transmission line structure is shown in the following figure with these parameters:

- Input parameters
  - **L**—Unit Length inductance (in various units)
  - **Rdc**—Unit length DC resistance (in various units)
  - **Rac**—Unit length skin-effect resistance (in various units)
  - **C**—Unit length capacitance (in various units)
  - **Gdc**—Unit length DC conductance (in various units)
  - **Gac**—Unit length AC conductance (in various units)
  - **Length**—Length of the coax (in various units)
  - **Freq**—Frequency where the Z0 (Impedance) and E-Eff (electrical length) are reported (in various units)
- Output parameters
  - **Z0**—Impedance at specified frequency **Freq** (Ohm)
  - **E-Eff**—Electrical length (in various units)

Figure 2-116: RLGC Transmission Line Channel Component Configuration



The channel component designer GUI can perform parameter unit conversion interactively. For example, you can change the length unit from mil to mm and the GUI will automatically compute the length value with the new unit.

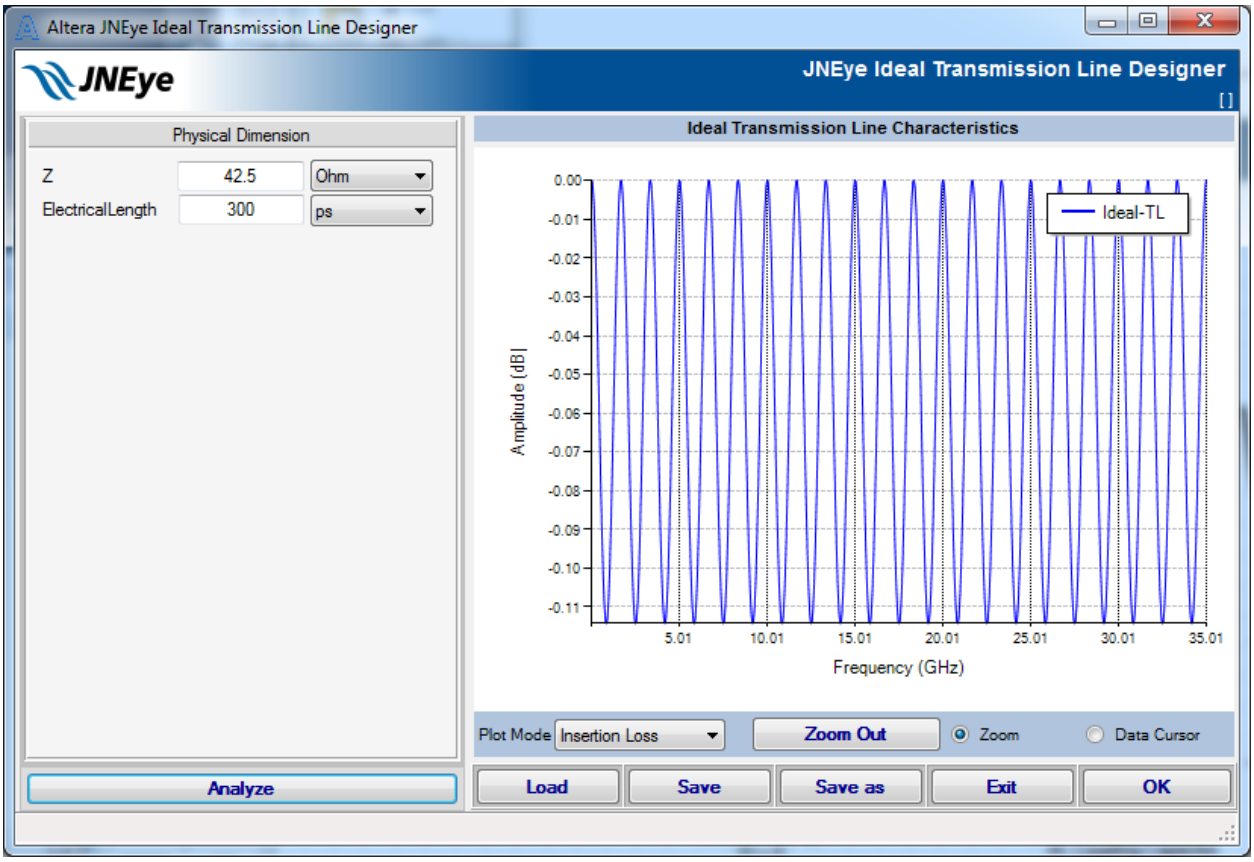
After entering the model parameters, click **Analyze** and Channel Designer will compute the frequency response of the current design. The integrated plotting engine can display the **insertion loss** or **return loss** characteristics. When you alter the model parameters, the GUI displays a message that indicates the channel characteristics may have changed. Click **Analyze** to redraw the channel characteristics. You can also **load** or **save** the component design for reuse in the future.

If you are satisfied with your design, click **OK** to save and close the component design GUI. If you click **Exit** or the **X** button of the window, the design will be discarded.

Ideal Transmission Line Component

- Input parameters
  - **Z0**—Target impedance (Ohm)
  - **Electrical length** (in various units)

Figure 2-117: Ideal Transmission Line Channel Component Configuration



The channel component designer GUI can perform parameter unit conversion interactively. For example, you can change the length unit from mil to mm and the GUI will automatically compute the length value with the new unit.

After entering the model parameters, click **Analyze** and Channel Designer will compute the frequency response of the current design. The integrated plotting engine can display the **insertion loss** or **return loss** characteristics. When you alter the model parameters, the GUI displays a message that indicates the channel characteristics may have changed. Click **Analyze** to redraw the channel characteristics. You can also **load** or **save** the component design for reuse in the future.

If you are satisfied with your design, click **OK** to save and close the component design GUI. If you click **Exit** or the **X** button of the window, the design will be discarded.

Via Component

In printed circuit board design, a via consists of two pads in corresponding positions on different layers of the board. The pads are electrically connected by a hole through the board. In JNEye Channel Designer, an analytical PCB Via model is constructed. A typical PCB via structure is shown in the following figure

and the analytical via model structure is shown in the figure after that. The via is configured with the following parameters:

- Input parameters
  - **Via**
    - **Impedance (Z3)** (Ohm)
    - **Electrical Length (td3)** (in various units)
  - **Pad 1**
    - **Capacitance (C1)** (in various units)
  - **Pad 2**
    - **Capacitance (C2)** (in various units)
  - **Via Stub 1**
    - **Impedance (Z1)** (Ohm)
    - **Electrical Length (td1)** (in various units)
    - **Termination (R1)** (in various units)
  - **Via Stub 2**
    - **Impedance (Z2)** (Ohm)
    - **Electrical Length (td2)** (in various units)
    - **Termination (R2)** (in various units)

Figure 2-118: PCB Via Channel Component Configuration

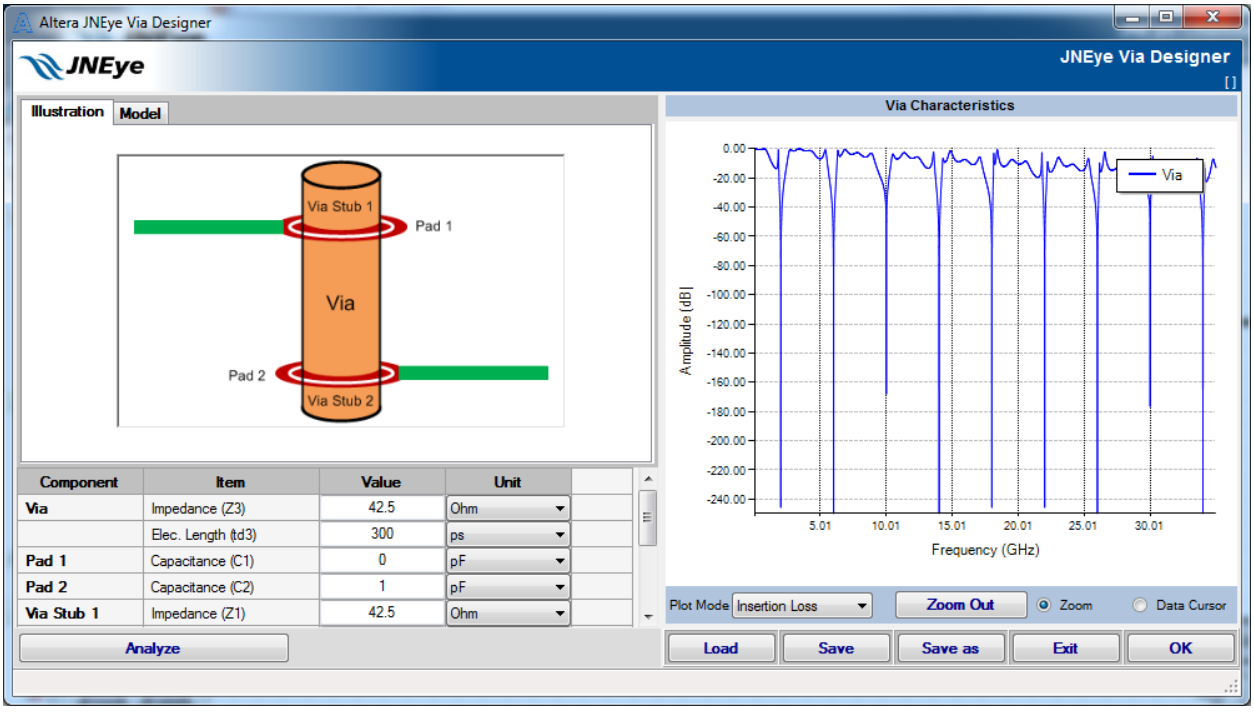
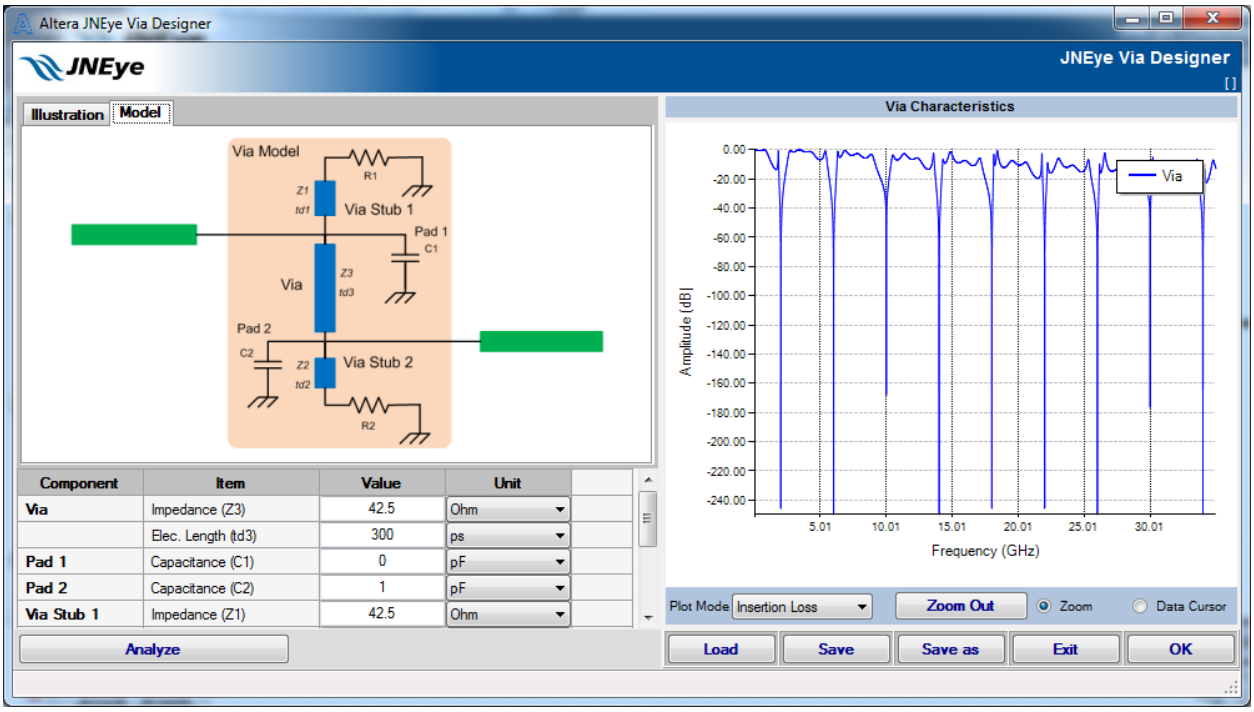


Figure 2-119: PCB Via Analytical Model Structure



The channel component designer GUI can perform parameter unit conversion interactively. For example, you can change the length unit from mil to mm and the GUI will automatically compute the length value with the new unit.

After entering the model parameters, click **Analyze** and Channel Designer will compute the frequency response of the current design. The integrated plotting engine can display the **insertion loss** or **return loss** characteristics. When you alter the model parameters, the GUI displays a message that indicates the channel characteristics may have changed. Click **Analyze** to redraw the channel characteristics. You can also **load** or **save** the component design for reuse in the future.

If you are satisfied with your design, click **OK** to save and close the component design GUI. If you click **Exit** or the **X** button of the window, the design will be discarded.

CHDE Component

JNEye Channel Design can use an existing JNEye Channel Designer project as a channel component. When you click the **CHDE** icon, a file browser opens and lets you select an existing Channel Designer configuration file.

Tutorial: PCI Express 8GT

3

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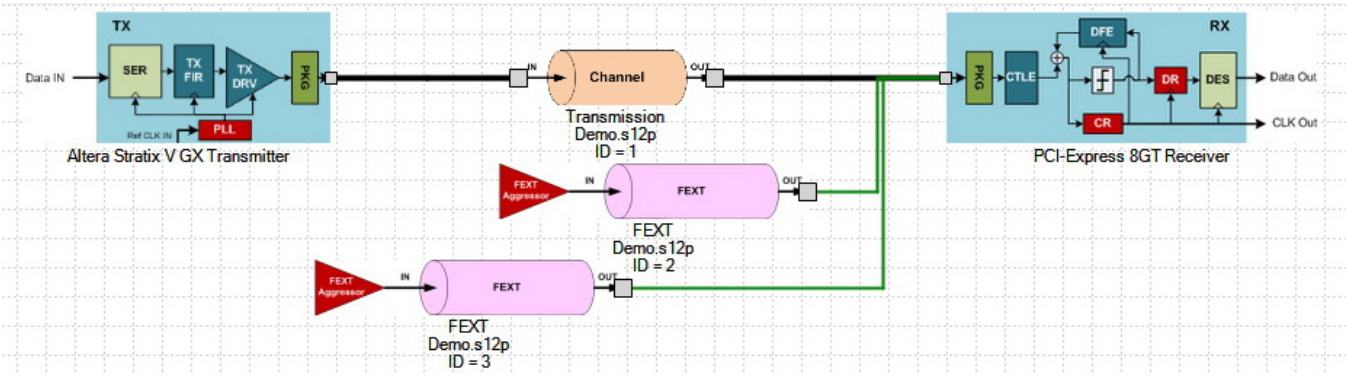
This tutorial uses JNEye to run a link simulation. This example and its associated channel models are provided with the JNEye distribution. The configuration file **Demo.jne** (included in the software distribution) contains the same link topology and a majority of the link settings discussed in this tutorial.

In this tutorial, a link that approximates a typical PCI-Express 8GT system with an Altera Stratix V GX transmitter and a generic PCI-Express 8GT receiver is built and simulated in JNEye. The following figure shows the link topology.

Note: This link configuration and simulation are for demonstration purposes. It is not intended for actual implementation. Consult Altera design guidelines for actual high-speed link design and implementation.

Figure 3-1: Example of PCI-Express 8GT Link Topology



Related Information

Link and Simulation Setting on page 2-6

The **Link and Simulation Setting** tab sets the global link parameters and simulation configurations.

Methodology

This simulation emulates an Altera Stratix V GX transmitter (with embedded package model), a PCI Express 8GT receiver (with embedded package model), and a ~18-inch backplane channel. Per PCI Express 8GT specifications, the link operates at 8 Gbps with a bit error rate (BER) < 10^{-12}. The transmitter must have a minimum differential output voltage of 800 mV and a rise/fall time of ~35 ps (at 0.8 V V_{OD}). In this simulation, the Stratix V GX transmitter is set to 800 mV V_{OD} (VOD level = 40). Additionally, the

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Stratix V GX transmitter has a 4-tap FIR to compensate for channel effects. The PCI Express 8G receiver has CTLE and a 1-Tap DFE per PCI-SIG definition.

To accomplish these goals, set up a transmitter model, a receiver model, and a link with the following parameters:

- Data rate: 8 Gbps
- Test pattern: PRBS-23
- BER target: BER < 10^{-12}
- Stratix V GX transmitter
  - V_{OD}: 800 mV (VOD Level = 40)
  - Edge rate: Per Stratix V GX characteristics
  - 4-Tap TX FIR (1 pre-tap and 2 post-taps)
  - Stratix V GX package model (embedded)
  - PLL: ATX (LC) set to low bandwidth
  - Output Jitter: Retrieved from the Altera Characterization Database (embedded in JNEye; contact your Altera representative to enable this function)
    - DCD = ~0.012 UI
    - BUJ = ~0.032 UI
    - RJ = ~1.00 ps_{RMS} (8 Gbps, BER < 10^{-12})
- Receiver
  - CTLE:
    - Programmable with 6 dB~12 dB boost at 4 GHz
    - Per PCI-SIG specifications
  - 1-tap DFE
  - PCI-SIG receiver package model (12-port S-parameter model from PCI-SIG)
  - CDR: Generic binary CDR with high loop bandwidth ~26 MHz
  - Receiver Jitter:
    - DJ = ~7 ps
    - RJ = ~1.55 ps_{RMS} (at BER < 10^{-12})

The ~18-inch backplane channel is described by a 12-port S-parameter model. The S-parameter is measured (or generated) with port configuration type 2, as shown in the following figure:

Figure 3-2: 12-port S-parameter with Port Configuration Type 2

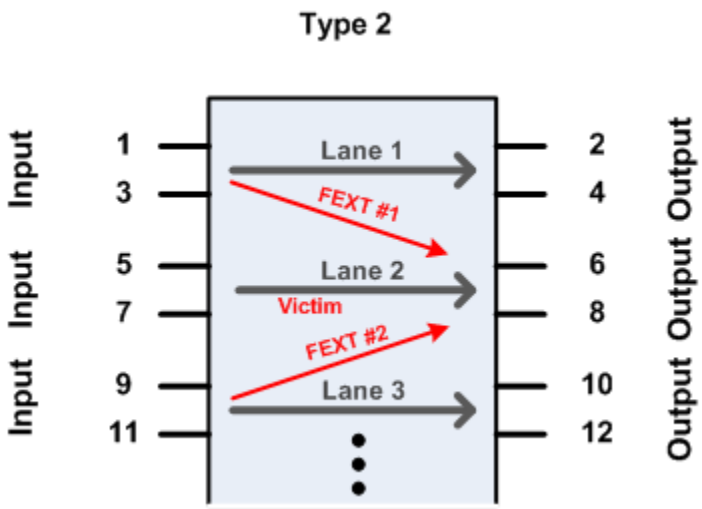
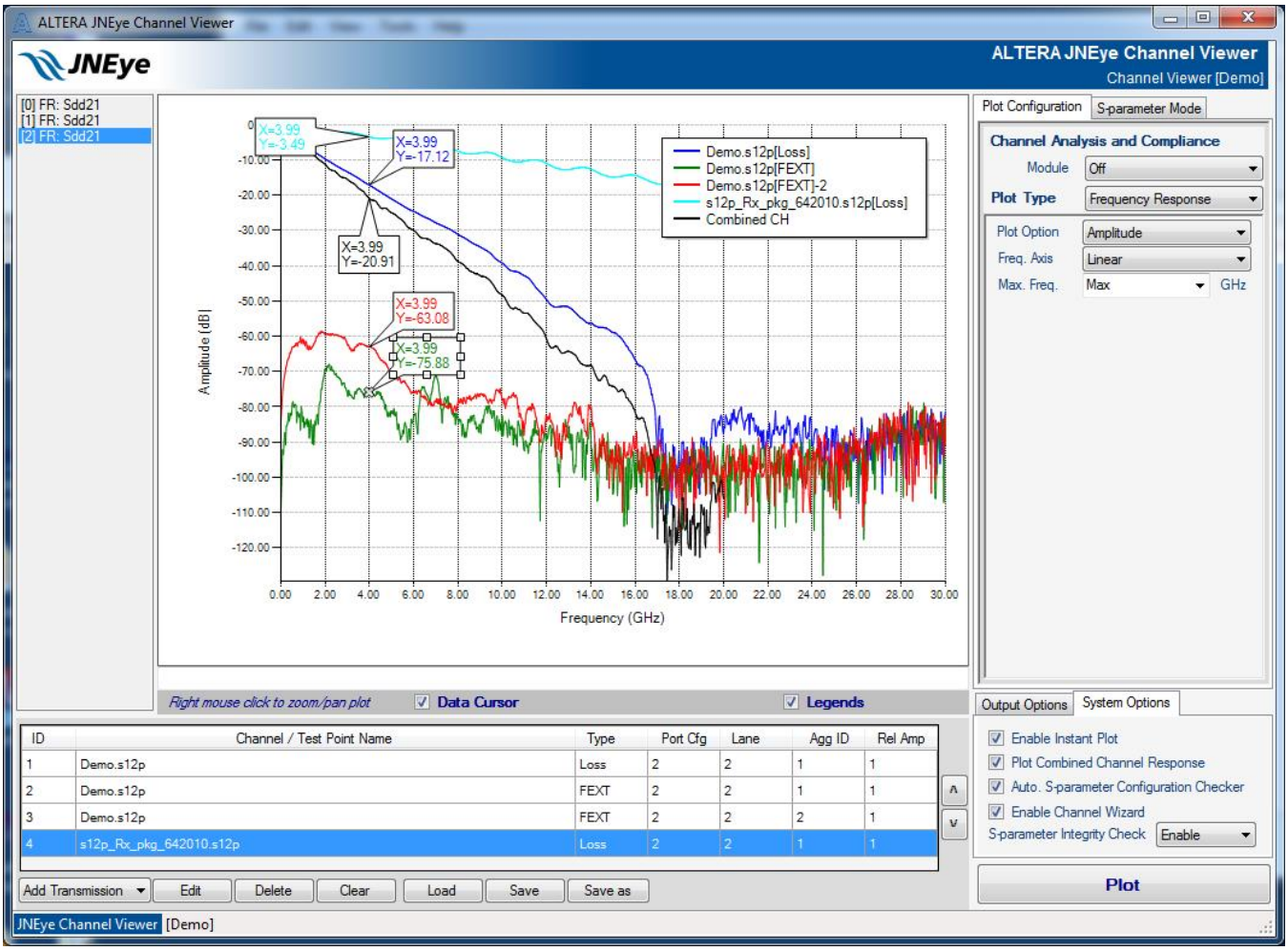


Figure 3-3: Channel Characteristics (Using JNEye Channel Viewer with Data Cursor Enabled)



The JNEye Channel Viewer shows that the backplane channel has approximately 17.15 dB loss at 4 GHz. The PCI-SIG RX package has 3.5 dB insertion loss at 4 GHz. The overall link has about 21 dB of loss (as shown in the Combined Channel black curve, not including Stratix V GX transmitter package) at 4 GHz, which requires heavy TX and RX equalizations to achieve the required BER target.

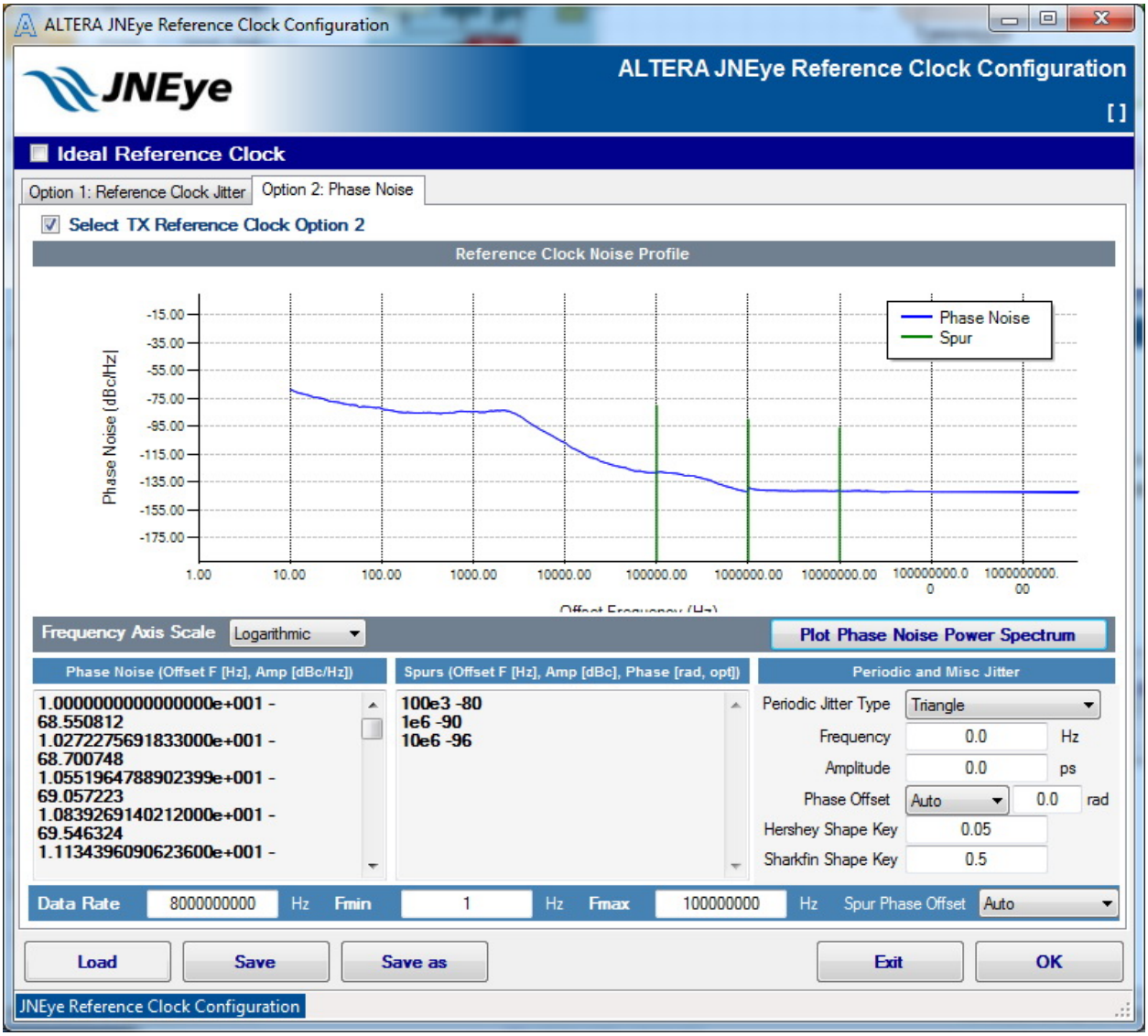
For comparative purposes, the following table and figure show a typical external 100 MHz transmitter reference clock with measured phase noise characteristics and spurs at three different frequencies.

Table 3-1: Phase Noise Characteristics

Phase Noise		Spurs	
Frequency	Phase Noise (dBc)	Frequency	Amplitude (dBc)
10 Hz	–68	100 KHz	–80
100 Hz	–82	1 MHz	–90

Phase Noise		Spurs	
Frequency	Phase Noise (dBc)	Frequency	Amplitude (dBc)
1 KHz	–84	10 MHz	–96
1 MHz and above	–140		

Figure 3-4: Transmitter Reference Clock Characteristics



The PLL in the Stratix V GX transmitter is enabled using ATX (LC) with low bandwidth configuration. The PLL effectively reduces the noise effects from the external reference clock.

Use the JNEye's link optimization algorithm to find the optimal equalization settings for both the transmitter and receiver. In this demonstration, you use the **CTLE => FIR => DFE** link optimization method.

Related Information

Link and Simulation Setting on page 2-6
The **Link and Simulation Setting** tab sets the global link parameters and simulation configurations.

Setup and Initialization

First, start JNEye. Input the following settings in the control module.

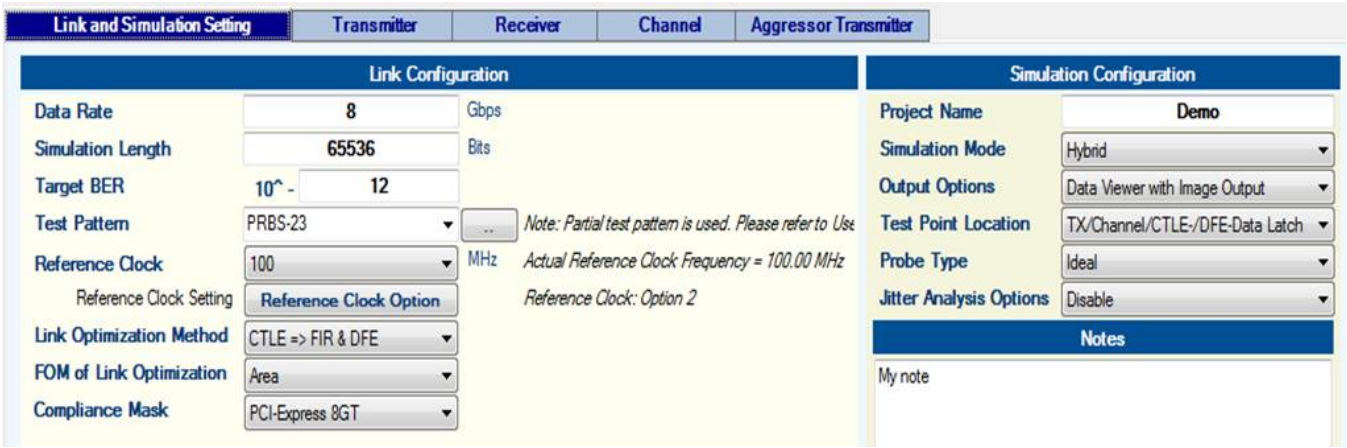
Related Information

Link and Simulation Setting on page 2-6
The **Link and Simulation Setting** tab sets the global link parameters and simulation configurations.

Setting Up the Control Module

Link and Simulation Tab

Figure 3-5: Link and Simulation Setting



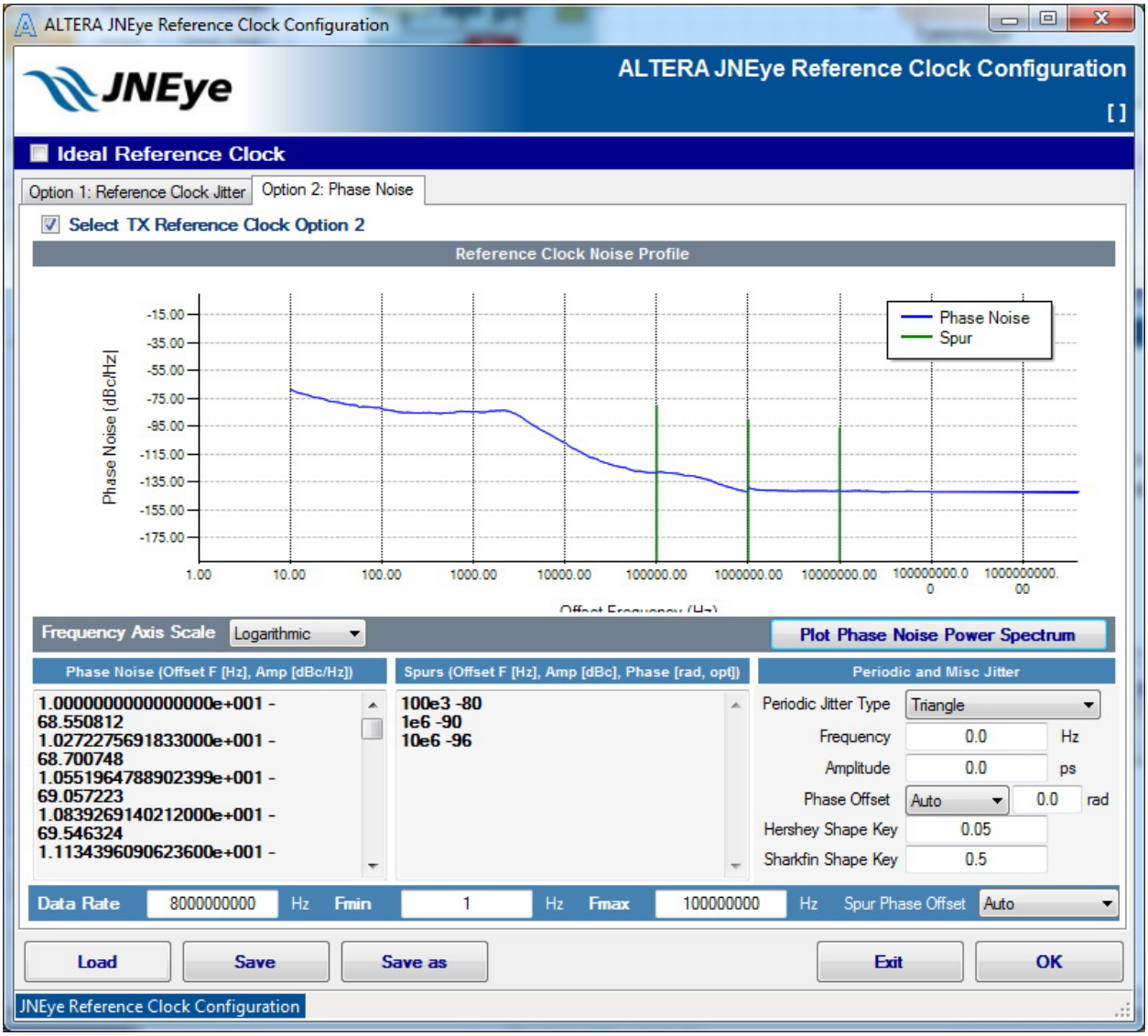
Set the following parameters in the **Link and Simulation Setting** tab:

- Data Rate: **8** (Gbps)
- Simulation Length: **65536** (Bits)
- Target BER: 10^ -**12**
- Test Pattern: **PRBS-23**
- Reference Clock: **100** (MHz)
- Link Optimization Method: **CTLE => FIR & DFE**
- FOM of Link Optimization: **Area**
- Compliance Mask: **PCI-Express 8GT**
- Project Name: **Demo**

- Simulation Mode: **Hybrid**
- Output Options: **Data Viewer with Image Output**. This option tells JNEye to generate image files (**.png**) for all output plots.
- Jitter Analysis Options: **Jitter Component**. This selection enables the jitter analysis function during the link simulation.

Click **Reference Clock Option**.

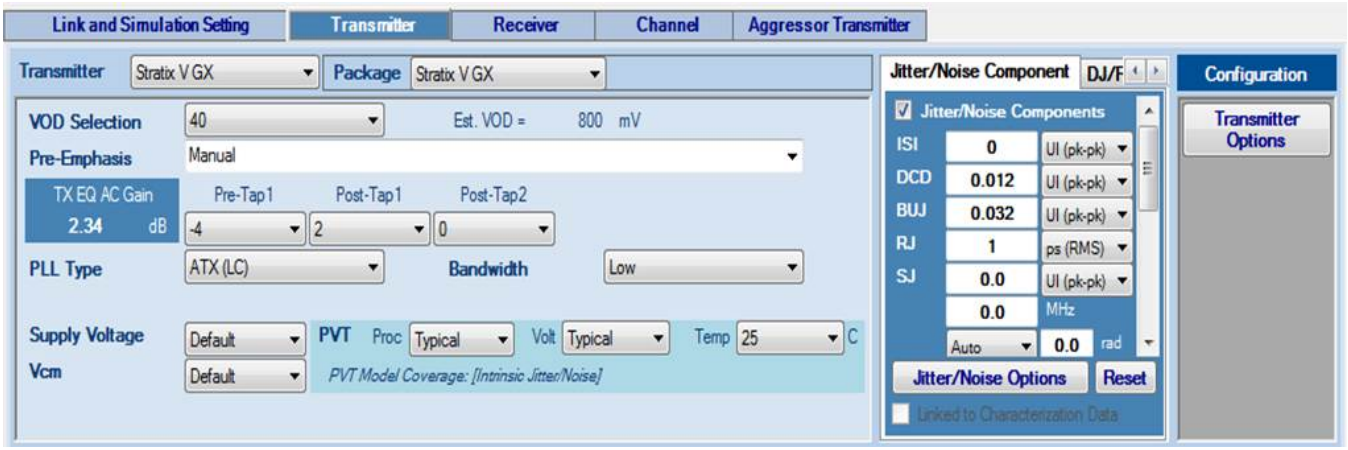
Figure 3-6: Reference Clock Configuration



- Turn off the **Ideal Reference Clock** option
- Click the **Option 2: Phase Noise** tab
- Turn on the **Select TX Reference Clock Option 2** option
- Type or copy the phase noise and spur data in the text boxes as shown in the above figure. The reference clock phase noise data can be found in the example configuration file **Demo.jne**.

Transmitter Tab

Figure 3-7: Transmitter Settings

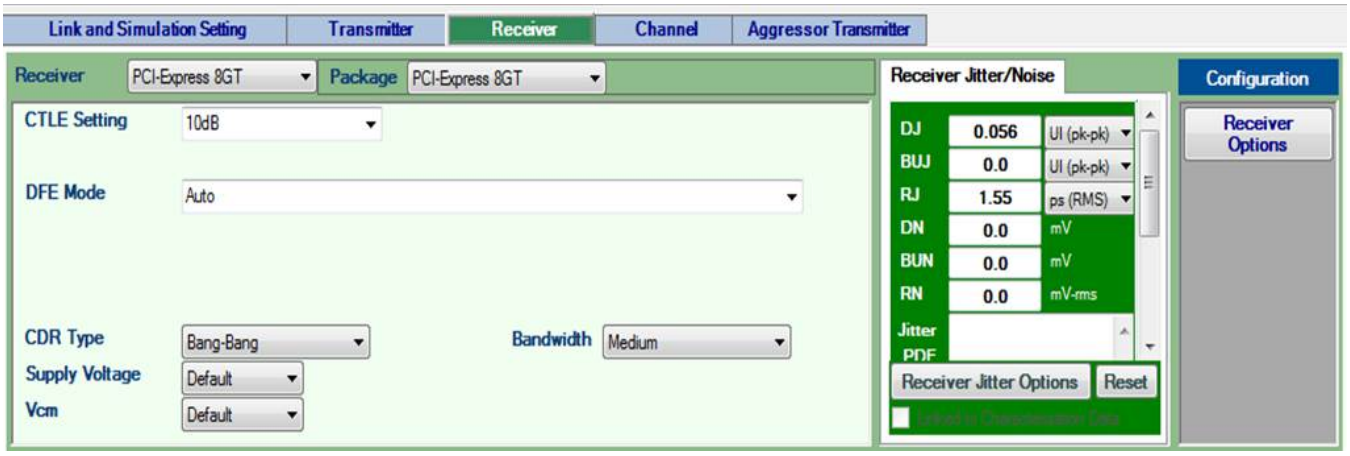


Set the following parameters in the Transmitter tab:

- Transmitter: **Stratix V GX**
- Package: **Stratix V GX**
- VOD Selection: **40** (~800 mV)
- Pre-emphasis: **Auto**
- PLL Type: **ATX (LC)**
- PLL Bandwidth: **Low**
- Jitter/Noise Component:
  - If the Altera Device Characterization Data Access function is enabled, click **Characterization Data Access**. (A message box appears. Read and close the message box.) Transmitter jitter figures are populated automatically and the jitter/noise modeling mode is selected.
  - If Altera Device Characterization Data Access is not available, manually type in the jitter numbers shown in the above figure. Note that the simulation results might differ slightly if the jitter data is from manual input.

Receiver Tab

Figure 3-8: Receiver Settings

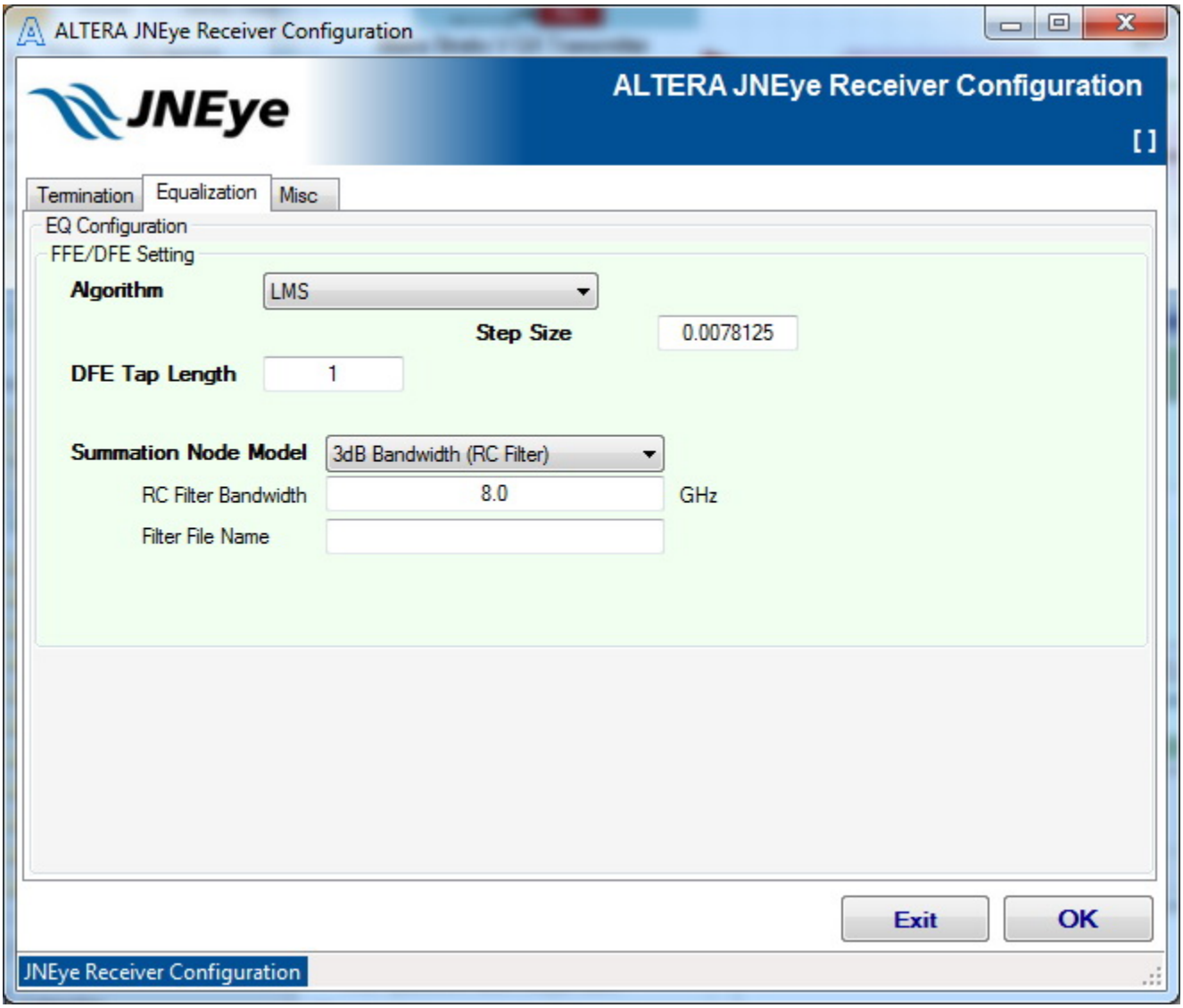


Set the following parameters in the Receiver tab:

- Receiver: **PCI-Express 8GT**
- Package: **PCI-Express 8GT**
- CTLE Setting: **Auto**
- DFE Mode: **Auto**
- CDR Type: **Bang-Bang**
- CDR Bandwidth: **Medium**
- PVT Process: **Typical**
- PVT Voltage: **Typical**
- PVT Temperature: **25** deg C
- DJ: **0.056** (UI, 7 ps)
- RJ: **1.55** ps (RMS) (key-in and then use pull-down menu to set RJ unit)

Click **Receiver Options**. In the Receiver Configuration window, click the **Equalization** tab. Set DFE Tap Length to **1** and Step Size to **0.0078125**.

Figure 3-9: Additional Receiver Configuration



Related Information

Link and Simulation Setting on page 2-6
The **Link and Simulation Setting** tab sets the global link parameters and simulation configurations.

Constructing the Channel

Next, construct the channel between the transmitter and receiver. In JNEye, the package models for the Stratix V GX transmitter and PCI-Express 8GT receiver are embedded. The transmitter and receiver packages are automatically included in the simulation.

JNEye supports **crosstalk modeling** capabilities. The channel engine and simulation engine can extract and interpret crosstalk characteristics from a single or a multi-lane S-parameter file and compute the crosstalk effects. In the channel list, crosstalk channels are assumed to run in parallel with the victim

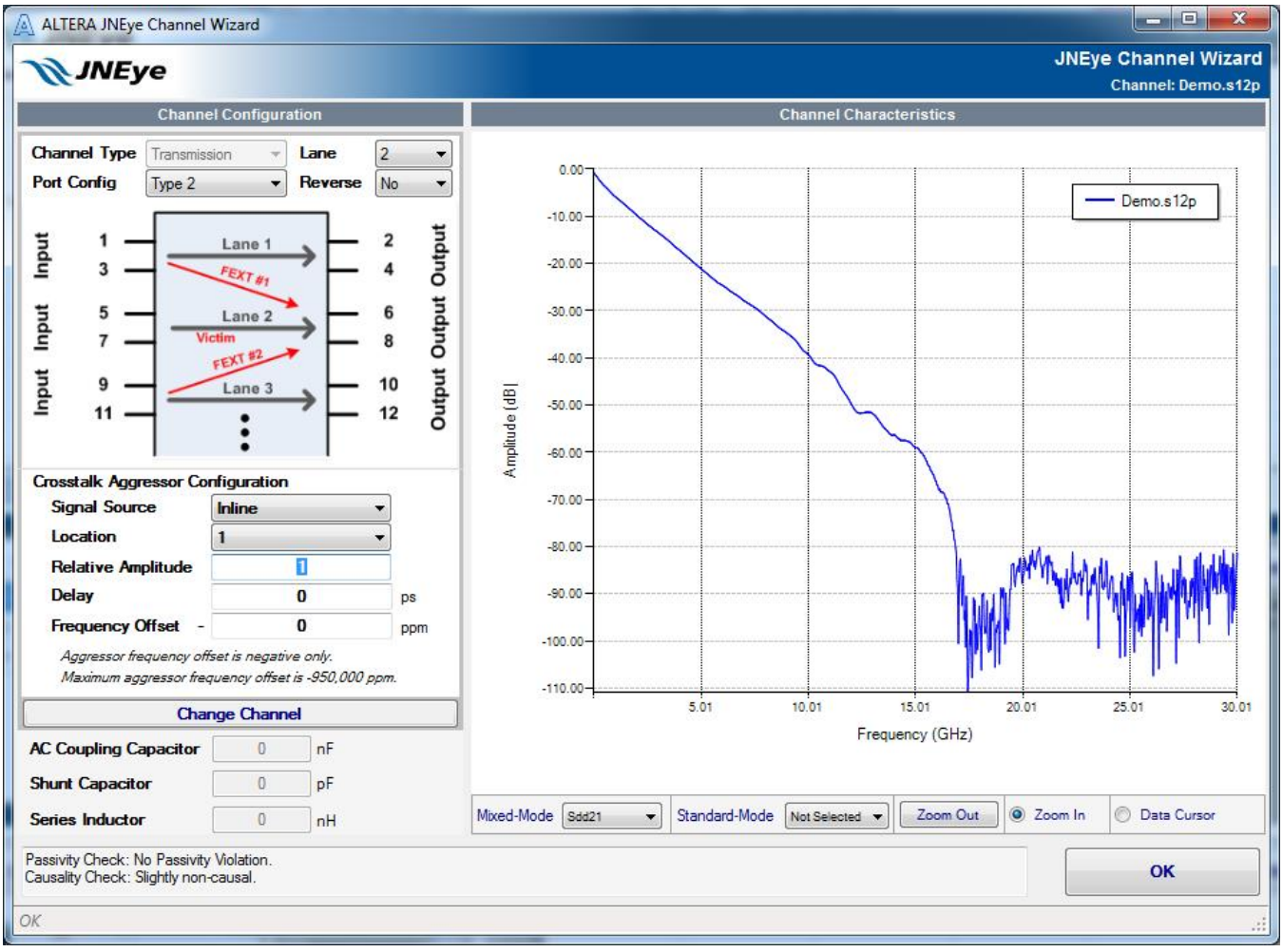
channel and the crosstalk noises are superimposed. This section describes how to set up crosstalk simulation in JNEye.

The backplane model is provided as a 12-port S-parameter. It consists of both insertion loss and crosstalk characteristics. However, JNEye requires you to add them one at a time (even if the loss and crosstalk characteristics are from the same multiple-lane S-parameter file). Therefore, you are going to insert three channel components during channel setup: one backplane victim channel and two backplane aggressor channels.

Perform the following steps to add a victim channel:

1. Click **Channel** in the Link Designer and select **Transmission**.
2. Use the file browser to locate the channel model file **Demo.s12p** and add it to the channel list as victim.
3. The JNEye Channel Wizard displays the Sdd21 characteristics of the middle lane (lane 2) in the 12-port S-parameter.
4. Click **OK** to close the Channel Wizard.
5. Place the channel icon in the Link Designer.

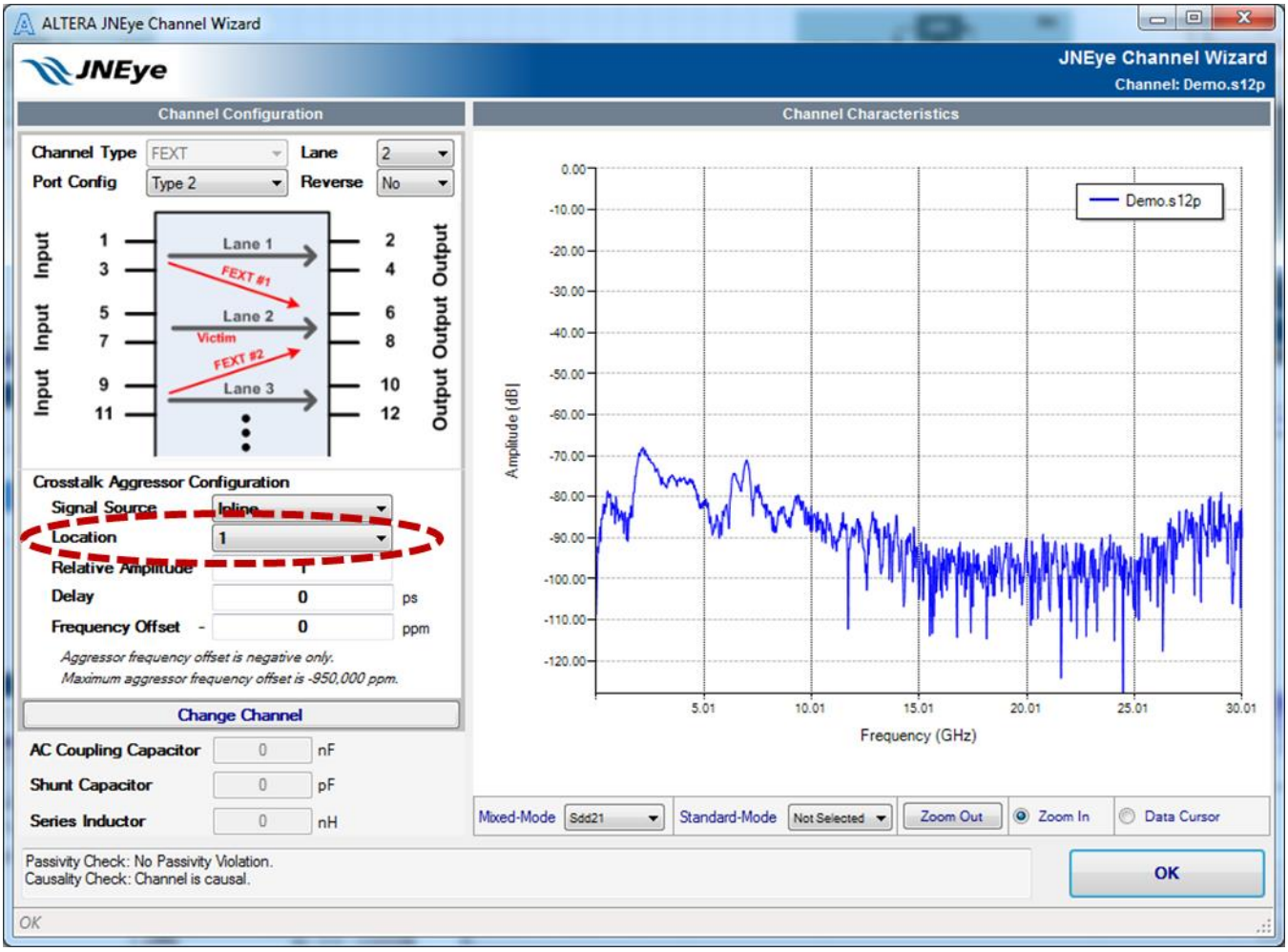
Figure 3-10: Configure Victim Channel with JNEye Channel Wizard



Perform the following steps to add the first crosstalk channel:

1. Click **Channel** in the Link Designer panel and select **Far-end Crosstalk (FEXT)**.
2. Use the file browser to locate the channel model file **Demo.s12p** and add it to the channel list as FEXT.
3. The JNEye Channel Wizard displays the FEXT #1 characteristic. Note that the **Crosstalk Aggressor Location 1** is selected in for this channel.
4. Click **OK** to close the Channel Wizard.
5. Place the channel icon in the Link Designer.

Figure 3-11: First Far-end Crosstalk Configuration in Channel Wizard

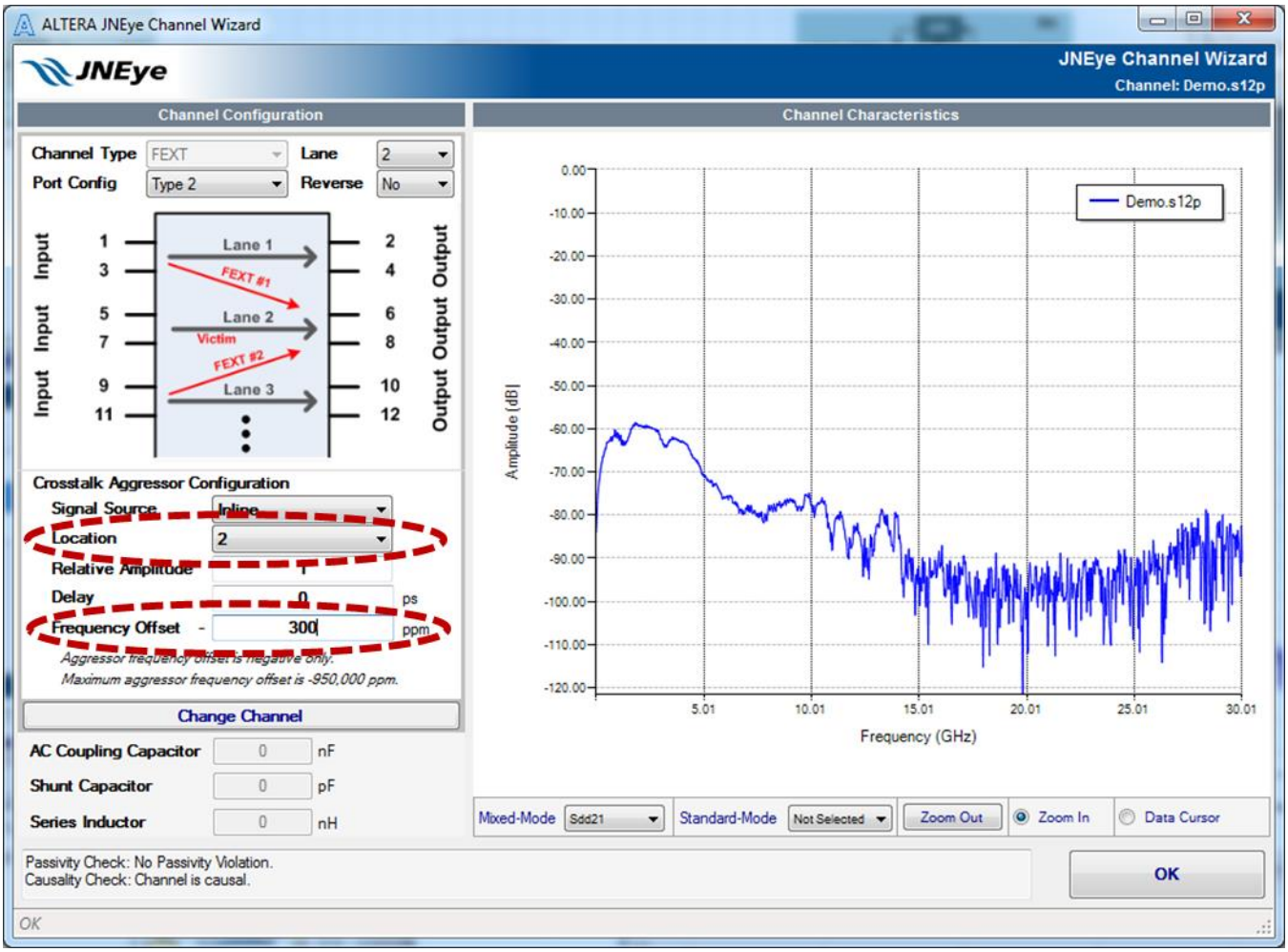


Perform the following steps to add the second crosstalk channel:

1. Click **Channel** in the Link Designer panel and select **Far-end Crosstalk (FEXT)**.
2. Use the file browser to locate the channel model file **Demo.s12p** and add it to the channel list as second FEXT.
3. The JNEye Channel Wizard displays the first FEXT channel characteristic by default.
4. Change the Crosstalk Aggressor Location to **2**. This tells JNEye to select the second FEXT in the12-port S-parameter.

5. Set the aggressor frequency offset to **300** ppm to emulate the phase shifting effect for this crosstalk noise source. This setting indicates the 2nd crosstalk is not frequency synchronous to the victim channel.
6. Click **OK** to close the Channel Wizard.
7. Place the channel icon in the Link Designer.

Figure 3-12: Second Far-end Crosstalk Configuration in Channel Wizard



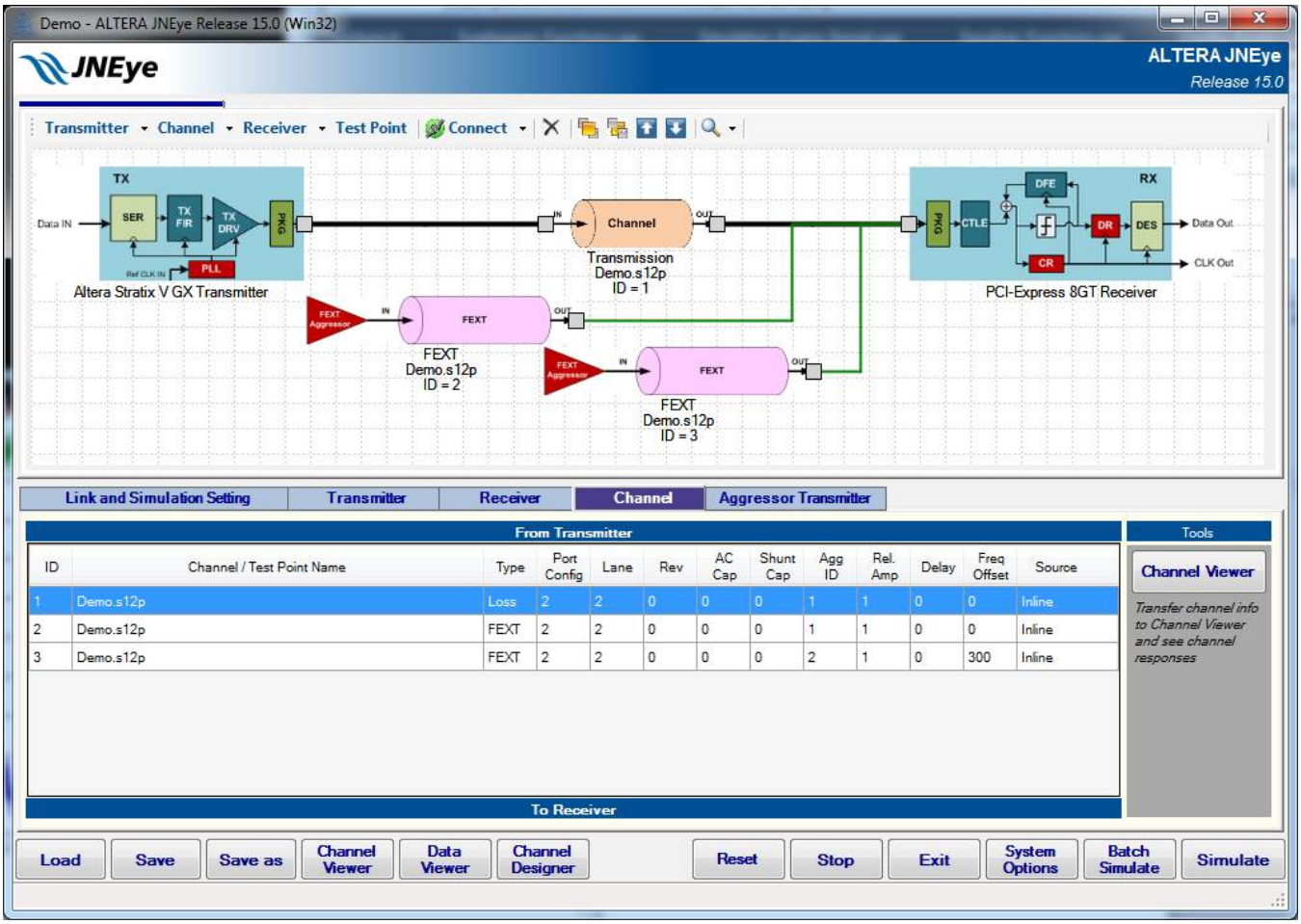
Related Information

Link and Simulation Setting on page 2-6
The **Link and Simulation Setting** tab sets the global link parameters and simulation configurations.

Completing the System

All the link components are now chosen and placed in the Link Designer. Click **Connect** in the Link Designer to begin connecting the components. Refer to the *Link and Simulation Setting* section for link construction in the Link Designer. The following figure shows the completed link system.

Figure 3-13: Complete Link Connection in Link Designer



The link configuration is complete. Use the **Save/Save as** buttons to save the configuration for later use.

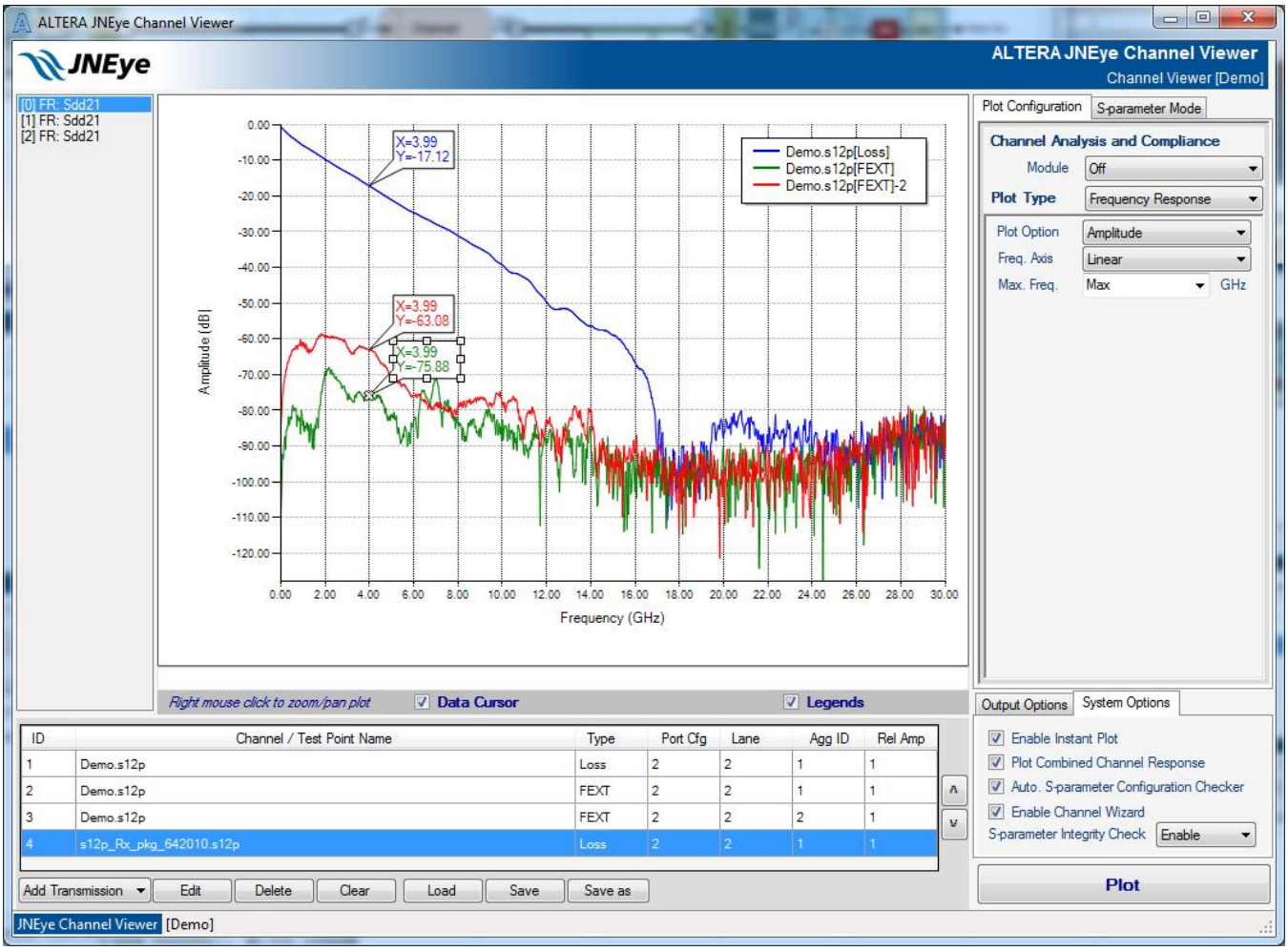
Related Information

Link and Simulation Setting on page 2-6
The **Link and Simulation Setting** tab sets the global link parameters and simulation configurations.

Analysis

Use the **Channel Viewer** to observe and analyze the channel characteristics. The **Channel Viewer** button is located on the right side of the Channel tab. This example shows the Sdd21 of the three channels you selected as well as the channel responses at test points and the overall channel. You can leave the **Channel Viewer** module open or close it by clicking **OK** or **Exit**.

Figure 3-14: Channel Characteristics of Victim and 2 FEXT Channels (with Data Cursor Enabled)



Start the channel simulation by clicking **Simulate** in the lower right corner of the JNEye Control Module. The JNEye Simulation Engine simulates all the models and generates eye diagrams at test points and inside the receiver (after CTLE and DFE).

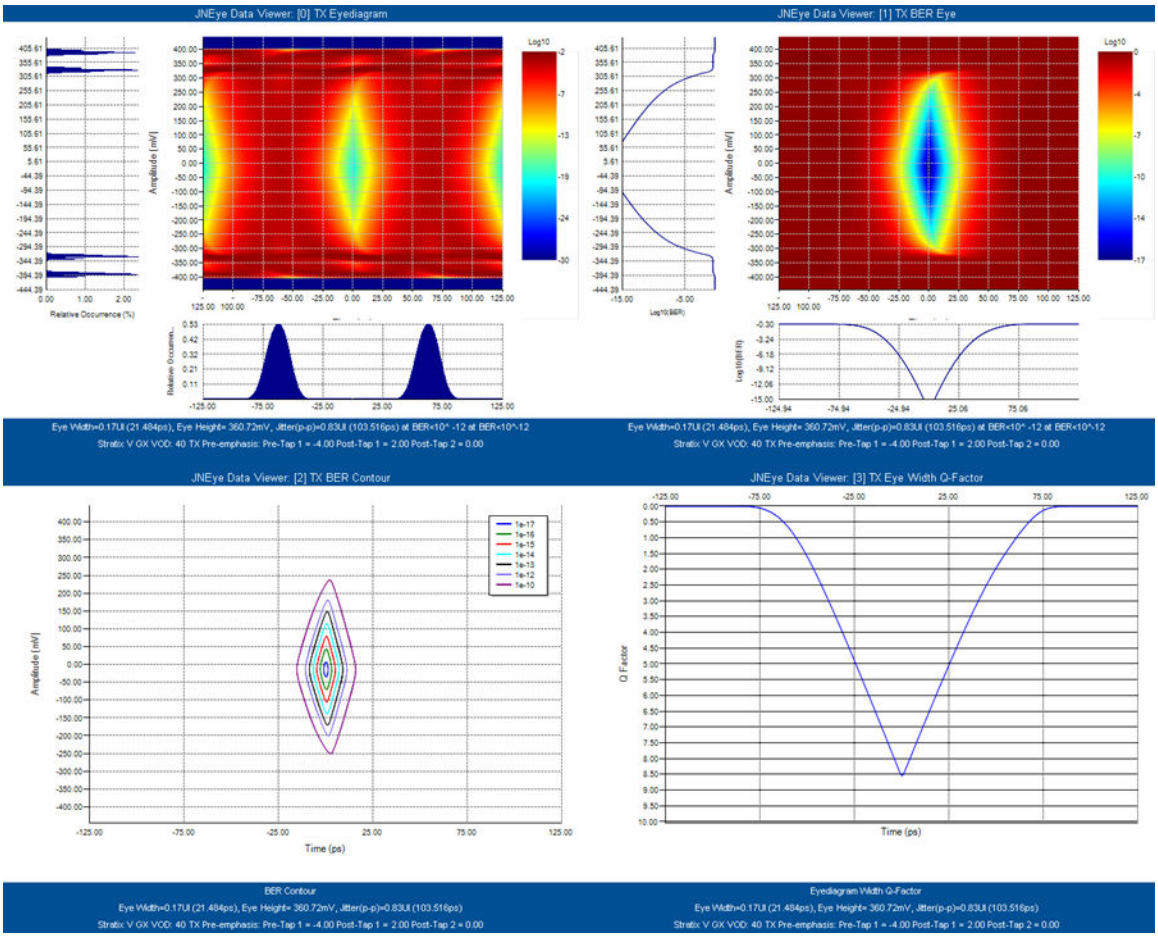
A goal of this tutorial was for JNEye to automatically find the optimal link setting for both transmitter and receiver. In the simulation time, the progress bar flashes, indicating the JNEye Simulation Engine is exploring the solution space. The link performance and result of the final setting is shown in a JNEye Data View.

At TX output, which is located after the Altera Stratix V GX transmitter output pin (after the TX package model), the results are shown in the following figure. JNEye found the optimal TX-FIR setting: **Pre-tap 1 = –4**, **Post-tap 1 = 2**, and **Post-tap 2 = 0**. The configured transmitter generates ~0.83 UI of jitter at BER = 10^{-12}. This set of TX outputs is measured with an ideal clock. In addition to the transmitter's intrinsic jitter, the reference clock's jitter and noise (recall that external reference clock phase noise and spurs in this simulation are filtered by the Stratix V GX 's PLL) are seen here.

- The first figure is a hybrid eye diagram that includes deterministic jitter and probability density function (PDF) because of unbounded jitter and noise sources.
- The second figure (top right) contains the cumulative distribution (CDF) eye diagram with BER bathtub curves (for both width and height in the eye diagram opening).
- The third plot (lower left) is a BER contour plot that shows the eye diagram opening area at various BER targets.
- The fourth plot shows Q-Factor curves, which are another representation of BER bathtub curve using Q-factor by assuming the noise/jitter is Gaussian.

With the Gaussian random jitter injected into the link, the BER bathtub and Q-Factor plots clearly show the effects where this unbounded jitter narrows the eye diagram width as the BER target reduces.

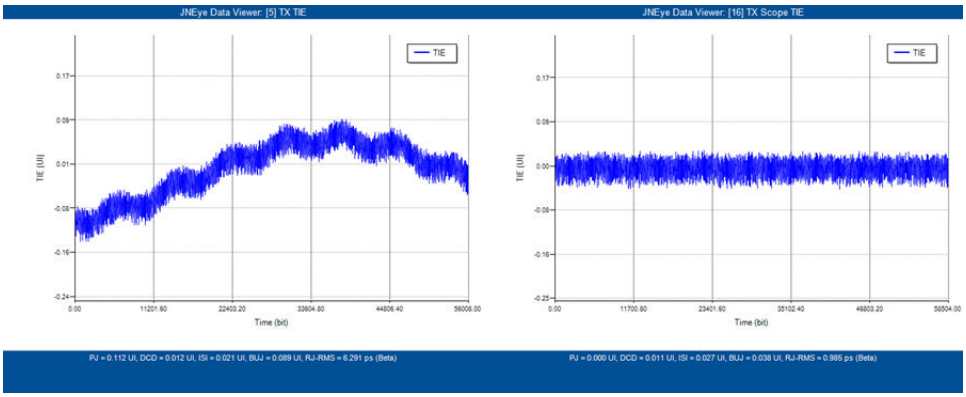
Figure 3-15: TX Output Hybrid Eye Diagrams and BER Analysis Measured with Ideal Clock


JNEye Data Viewer: [0] TX Eyediagram
JNEye Data Viewer: [1] TX BER Eye
JNEye Data Viewer: [2] TX BER Contour
JNEye Data Viewer: [3] TX Eye Width Q-Factor
Time (ps)
Q Factor
BER Contour
Eyediagram Width Q-Factor

The second set of TX outputs are measured with the golden CDR, which has a loop bandwidth of 1/1667 of the data rate. This set of outputs reflects the common lab scope measurement. With the golden CDR in place, the low frequency jitter and noise, which are included in phase noise and spurs, are tracked.

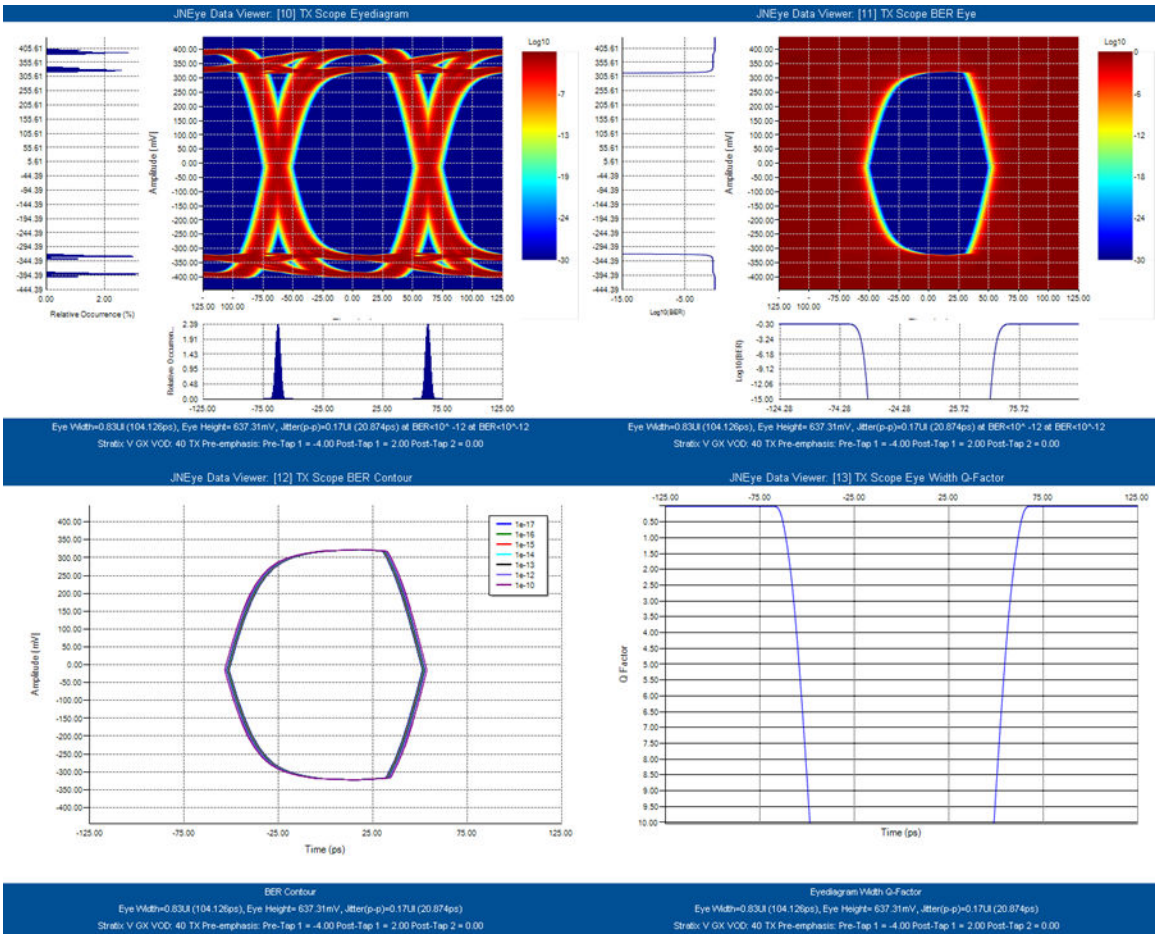
The following figure shows the Time Interval Error (TIE) plots before and after the golden CDR. With reference to the ideal clock (that is, before the golden CDR), the low frequency sinusoidal jitter from the reference clock characteristics can be clearly observed in the plot on the left. After the golden CDR, those low frequency sinusoidal jitters are tracked as shown in the plot on the right. The figure also shows the jitter components results that reflect the effects of the golden CDR (Beta feature).

Figure 3-16: Transmitter Output TIE (Time Interval Error) Plots with Reference Clock Phase Noise and Spurs Before and After the Golden CDR



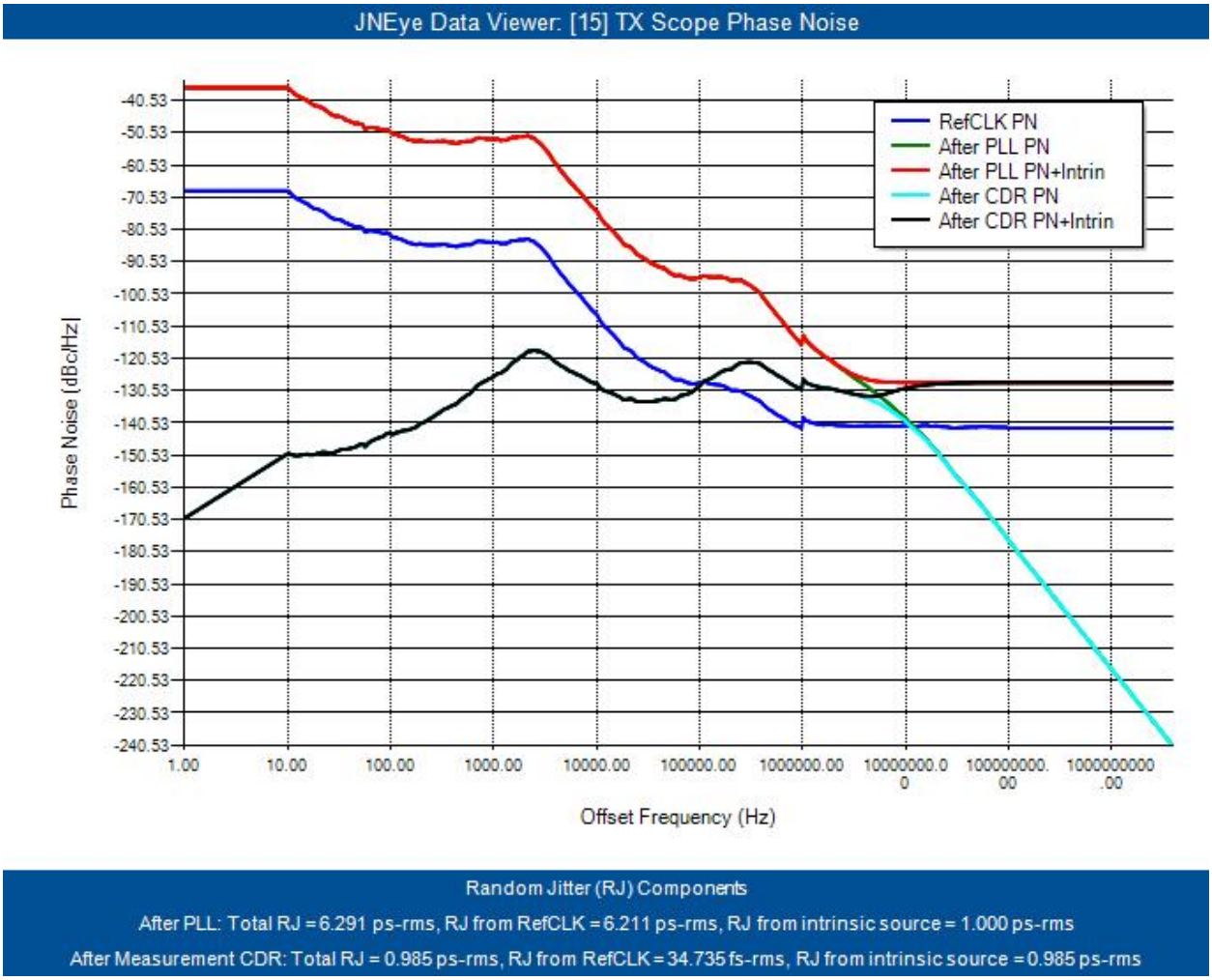
In the following figure, the transmitter output jitter, which includes transmitter intrinsic jitter and PLL filtered reference clock jitter, is about 0.17 UI at BER 10^{-12}.

Figure 3-17: Transmitter Scope Output Measured with Golden CDR


JNEye Data Viewer: [10] TX Scope Eyediagram
JNEye Data Viewer: [11] TX Scope BER Eye
JNEye Data Viewer: [12] TX Scope BER Contour
JNEye Data Viewer: [13] TX Scope Eye Width Q-Factor
Amplitude [mV]
Time (ps)
Q Factor

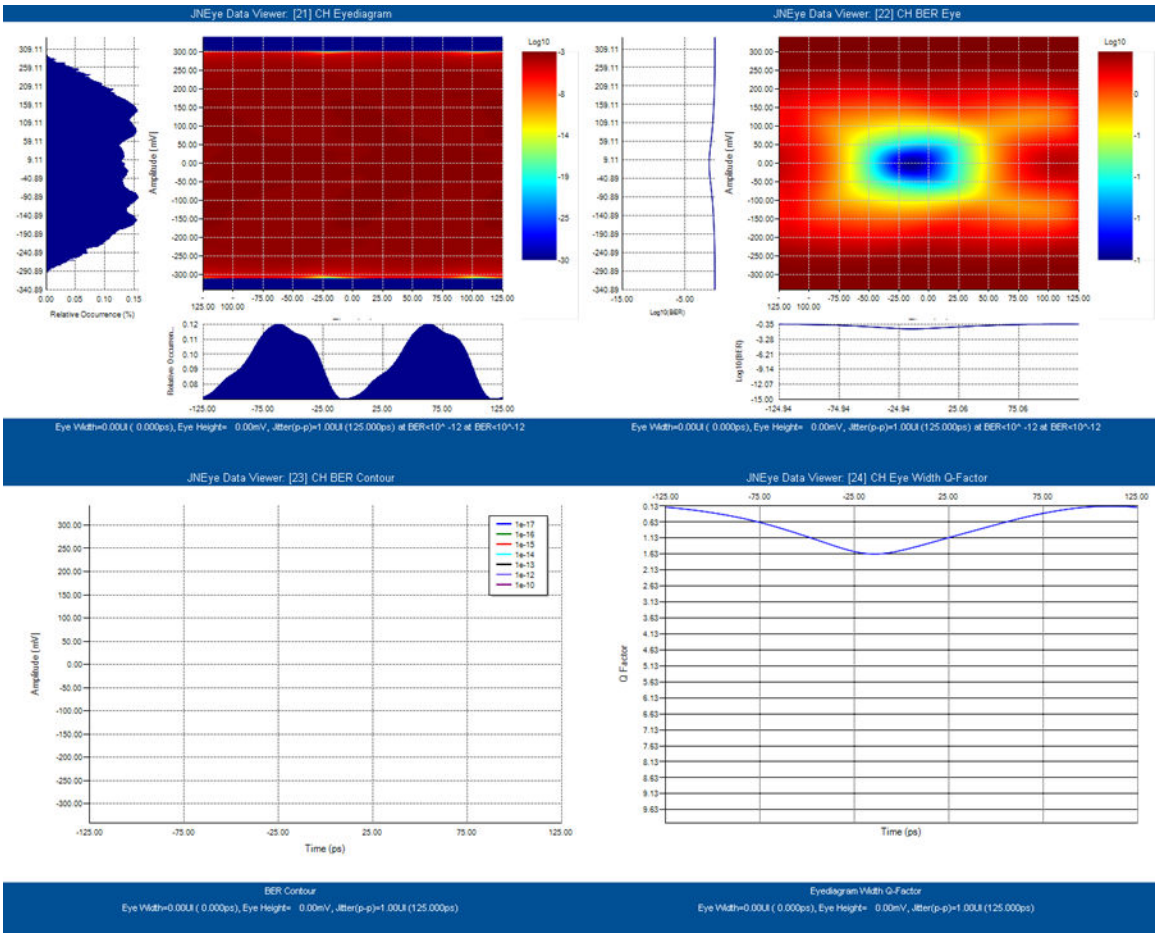
When you enable a PLL in a transmitter, the reference clock's phase noise is shaped and filtered with the PLL's response. The following figure shows the characteristics of phase noise at the output of the reference clock (blue), after the transmitter PLL (green), after the transmitter PLL plus the transmitter's intrinsic jitter (red), after the Golden CDR (most likely in a scope, cyan), and after the Golden CDR with transmitter's intrinsic jitter (black). The associated random jitter from the phase noise power spectrum at each of the above stages are calculated and displayed in the text below the plot.

Figure 3-18: Reference Clock Phase Noise Characteristics Before and After TX PLL



At the channel output, which is located at the end of backplane channel with crosstalk, the eye diagram is largely closed because of the large channel loss from the TX package and the backplane.

Figure 3-19: Channel Output Hybrid Eye Diagrams and BER Analysis


JNEye Data Viewer: [21] CH Eyediagram
JNEye Data Viewer: [22] CH BER Eye
JNEye Data Viewer: [23] CH BER Contour
JNEye Data Viewer: [24] CH Eye Width Q-Factor
Time (ps)
BER Contour
Eyediagram Width Q-Factor

The CTLE is a PCI-Express 8GT CTLE behavior model output stage. The JNEye's link optimization algorithm has identified the optimal gain setting at 10 dB level. Similar to the TX output case, when the receiver CDR is enabled or included in the simulation, two sets of CTLE outputs are shown. The first set of outputs is with the ideal clock and the second one is with the CDR recovered clock. The total jitter is 1 UI (at BER < 10^{-12}, with ideal clock) or 0.54 UI (with CDR recovered clock). The eye diagram opening height is 0 mV (with ideal clock) and 41 mV (with recovered clock). The eye diagram opening is marginal to PCI-Express 8GT requirements. Therefore, further equalization of the signal with DFE is needed.

Figure 3-20: CTLE Output Hybrid Eye Diagram and BER Analysis with Ideal Clock

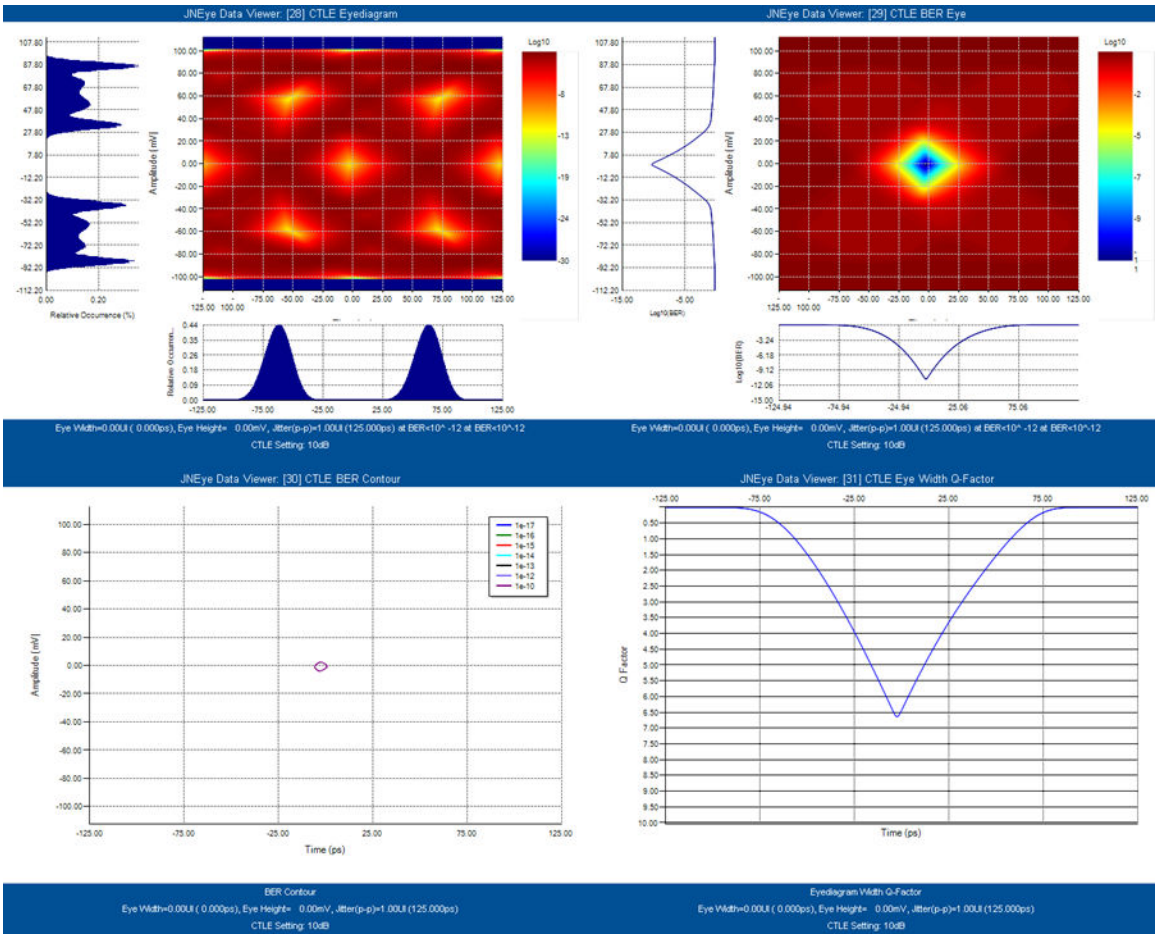
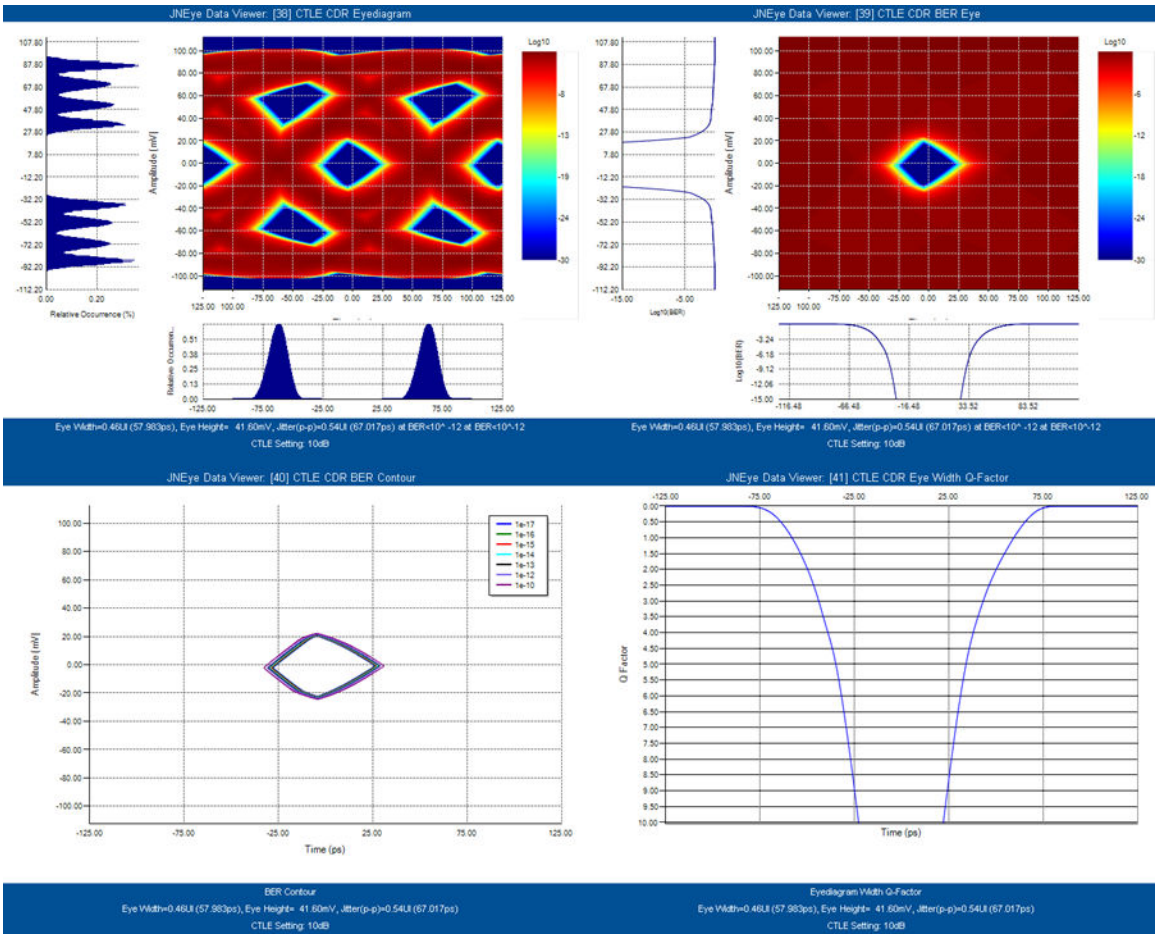
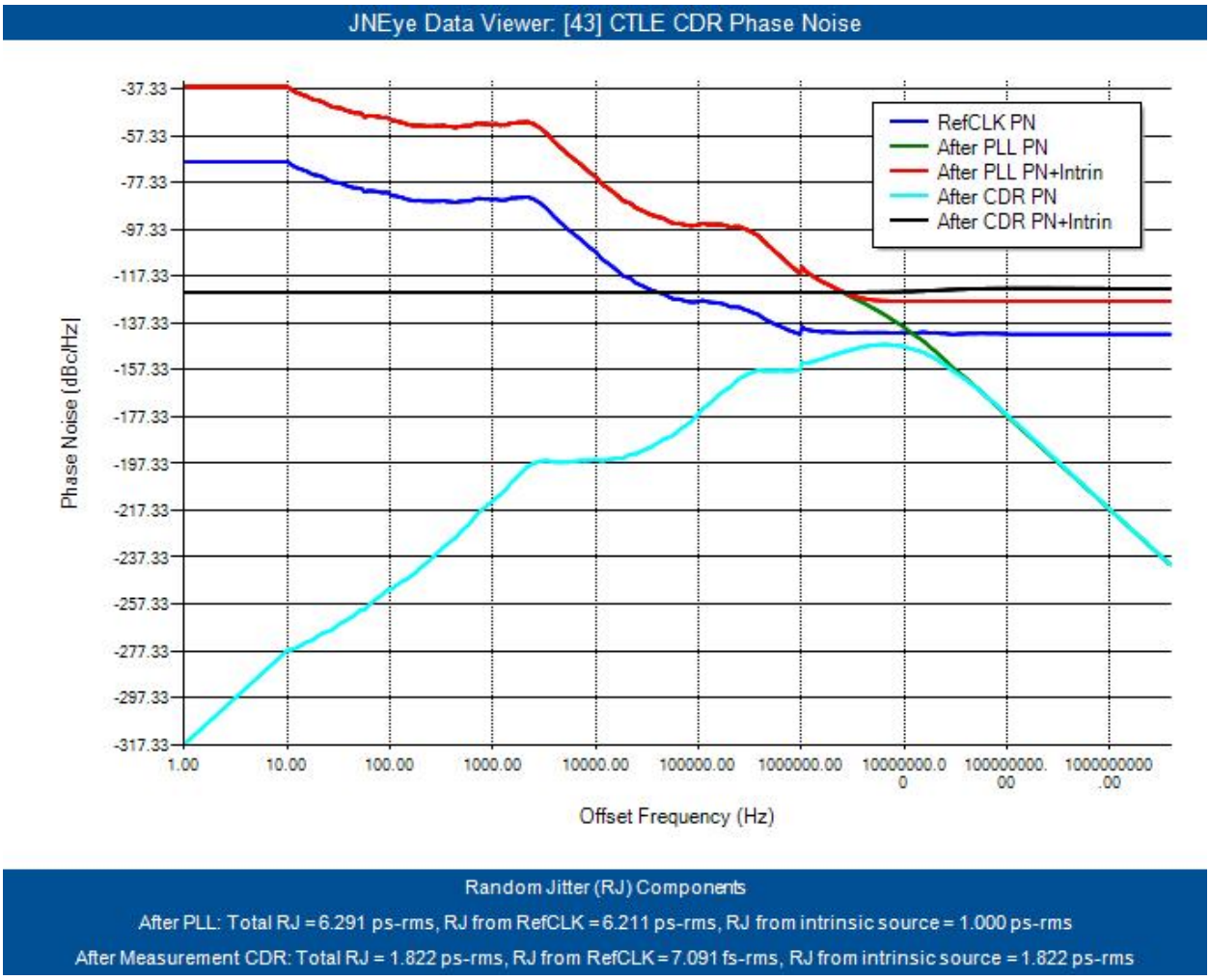

JNEye Data Viewer: [28] CTLE Eyediagram
JNEye Data Viewer: [29] CTLE BER Eye
JNEye Data Viewer: [30] CTLE BER Contour
JNEye Data Viewer: [31] CTLE Eye Width Q-Factor
Time (ps)
Q Factor
BER Contour
Eyediagram Width Q-Factor

Figure 3-21: CTLE Output Hybrid Eye Diagram and BER Analysis with CDR Recovered Clock


JNEye Data Viewer: [38] CTLE CDR Eyediagram
JNEye Data Viewer: [39] CTLE CDR BER Eye
JNEye Data Viewer: [40] CTLE CDR BER Contour
JNEye Data Viewer: [41] CTLE CDR Eye Width Q-Factor
Time (ps)
Q Factor
BER Contour
Eyediagram Width Q-Factor

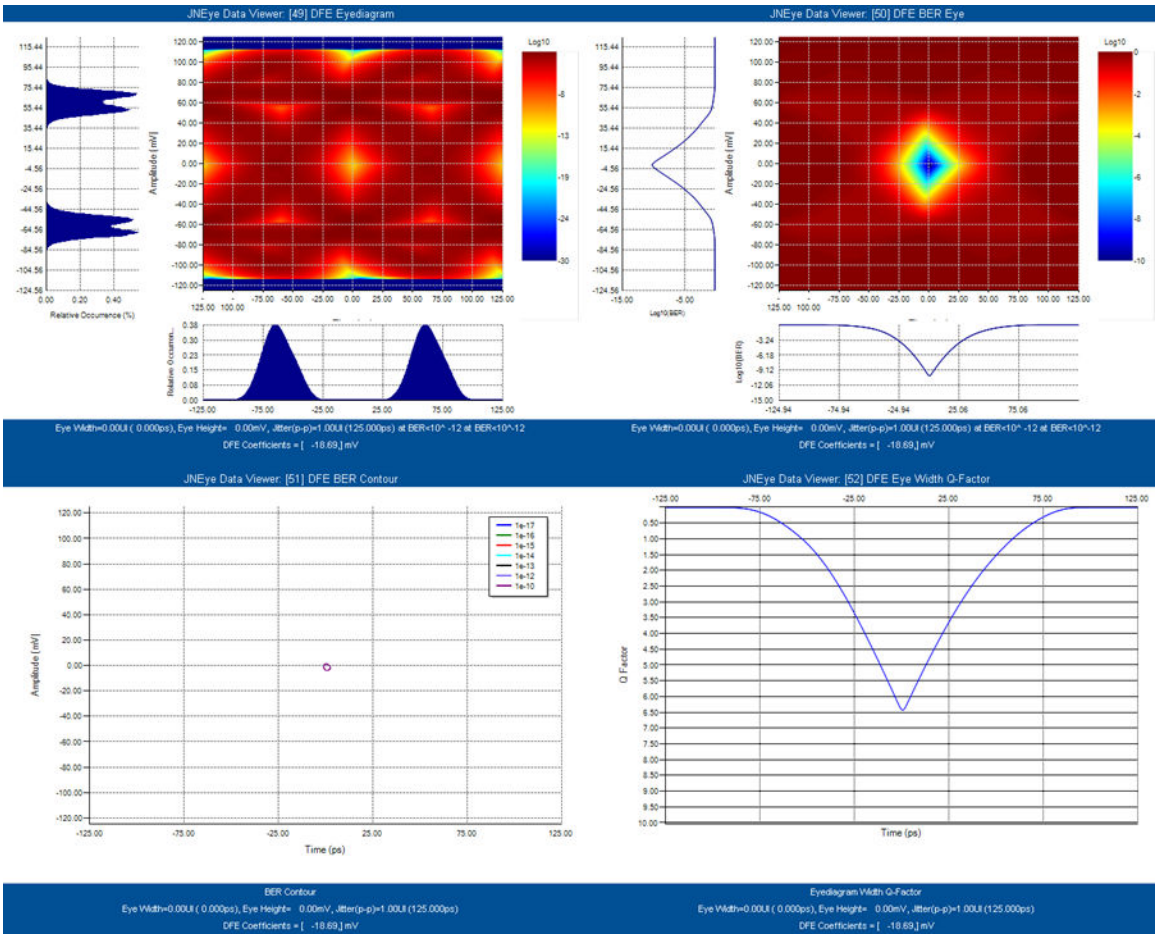
When you enable CDR in a receiver, the reference clock's phase noise is shaped and filtered with the CDR's response. The following figure shows the characteristics of phase noise at the output of the reference clock (blue), after the transmitter PLL (red), after the transmitter PLL plus the transmitter's intrinsic jitter (red), after the RX CDR (cyan), and after the RX CDR with transmitter and receiver's intrinsic jitter (black). The associated random jitter from the phase noise power spectrum at each of the above stages was calculated and displayed in the text below the plot.

Figure 3-22: Phase Noise of Reference Clock and Its Transitions through PLL and CDR



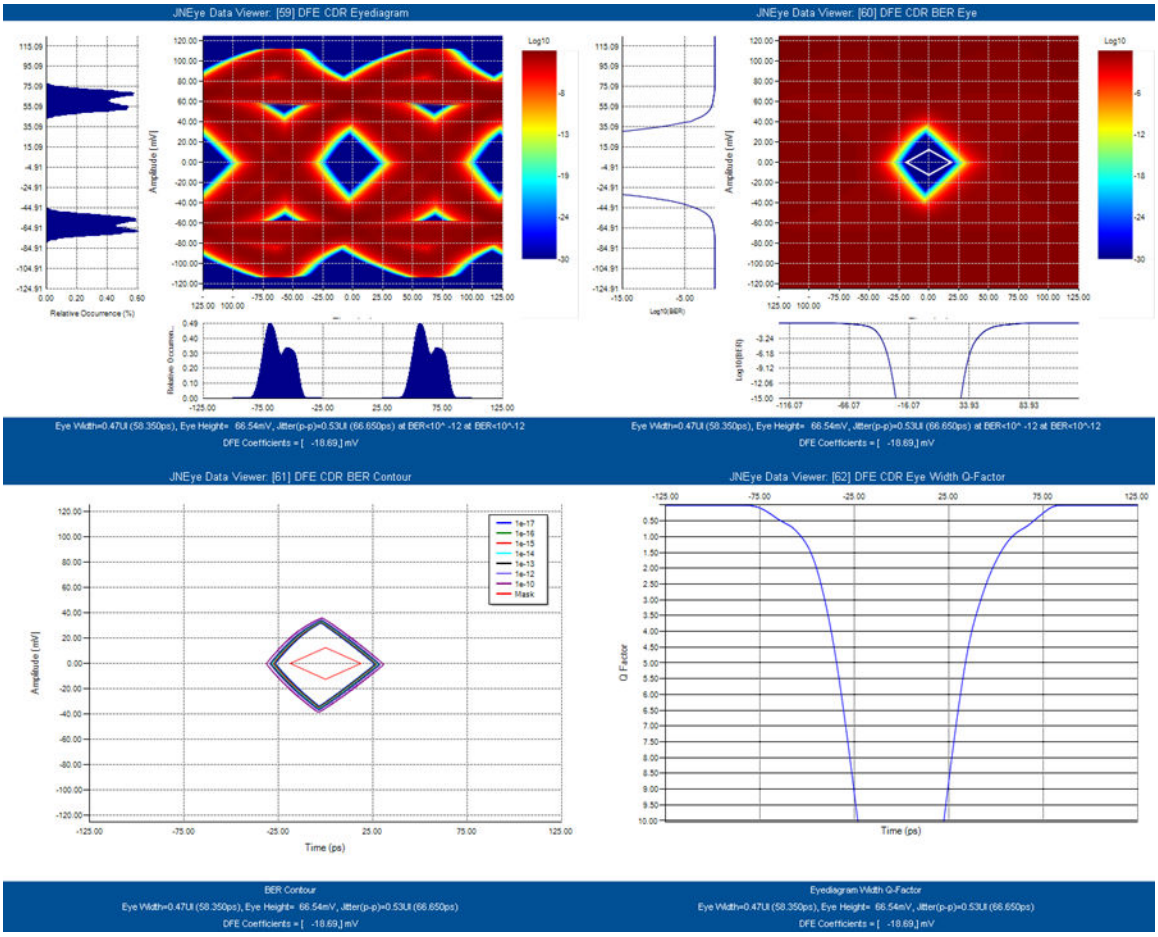
At the output of the PCI-Express 8G receiver's 1-Tap DFE, the following figures show that the DFE has further opened the eye diagram with a total jitter of 1 UI (at BER < 10^{-12}, with ideal clock and sinusoidal jitter from the transmitter reference clock) and 0.53 UI (with CDR recovered clock) and eye diagram opening height of 0 mV (with ideal clock) and 66 mV (with recovered clock). The BER bathtub curve and contour show good behavior and successfully meet the PCI-Express 8GT RX requirements (TJ < 0.7 UI and eye diagram height > 25 mV; refer to PCI-Express Base Specification 4.3).

Figure 3-23: TP4 Hybrid Eye Diagram and BER Analysis Measured with Ideal Clock


JNEye Data Viewer: [49] DFE Eyediagram
JNEye Data Viewer: [50] DFE BER Eye
JNEye Data Viewer: [51] DFE BER Contour
JNEye Data Viewer: [52] DFE Eye Width Q-Factor
Time (ps)
Q Factor
BER Contour
Eyediagram Width Q-Factor

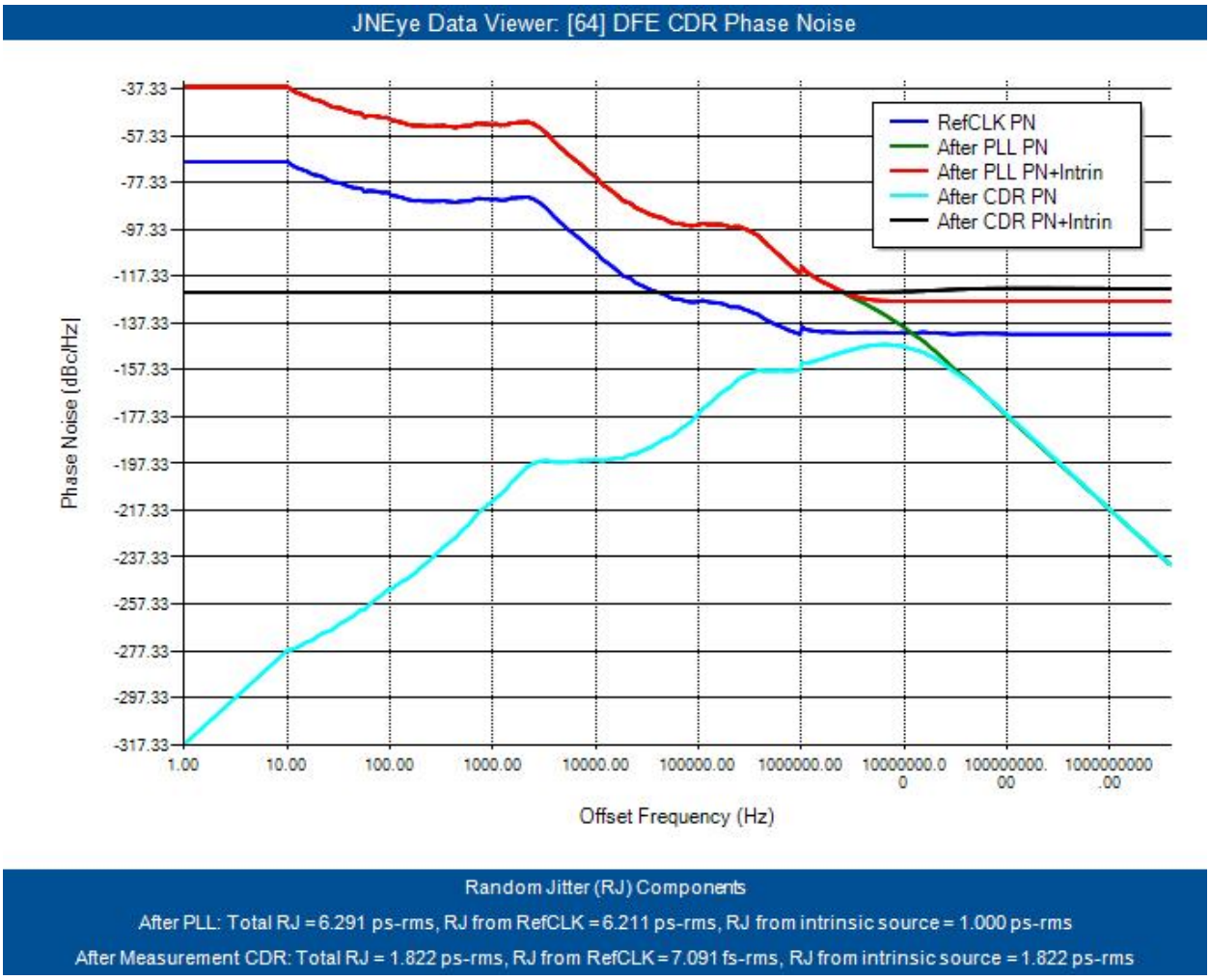
The PCI-Express 8GT eye diagram mask is shown in the following figure to see the margins to the specification limits.

Figure 3-24: TP4 Hybrid Eye Diagram Measured with CDR Recovered Clock and PCI-Express 8GT Receiver Eye Diagram Mask


JNEye Data Viewer: [59] DFE CDR Eyediagram
JNEye Data Viewer: [60] DFE CDR BER Eye
JNEye Data Viewer: [61] DFE CDR BER Contour
JNEye Data Viewer: [62] DFE CDR Eye Width Q-Factor
Time (ps)
Q Factor
BER Contour
Eyediagram Width Q-Factor

When you enable a CDR in a receiver, the reference clock's phase noise is shaped and filtered with the CDR's response. The following figure shows the characteristics of phase noise at the output of the reference clock (blue), after transmitter PLL (red), after transmitter PLL plus transmitter's intrinsic jitter (red), after RX CDR (cyan), and after RX CDR with transmitter and receiver's intrinsic jitter (black). The associated random jitter from the phase noise power spectrum at each of the above stages are calculated and displayed in the text below the plot.

Figure 3-25: Phase Noise of Reference Clock and Its Transitions through PLL and CDR



These examples demonstrated how to use JNEye to set up a serial link and evaluate its link performance. JNEye allows you to:

- Configure a link
- Configure an external reference clock
- Configure a transmitter and receiver
- Configure a channel
- Configure and model jitter and noise sources
- Derive accurate jitter figures for Altera devices from the Altera JBE database
- Load and save a link configuration
- Observe the channel characteristics
- Set up test points within the link
- Compute and observe an eye diagram
- Perform BER analysis

Related Information

Link and Simulation Setting on page 2-6
The **Link and Simulation Setting** tab sets the global link parameters and simulation configurations.

Tutorial: 28 Gbps OIF VSR Link with Arria 10 GT

4

2015.05.04

UG-1146

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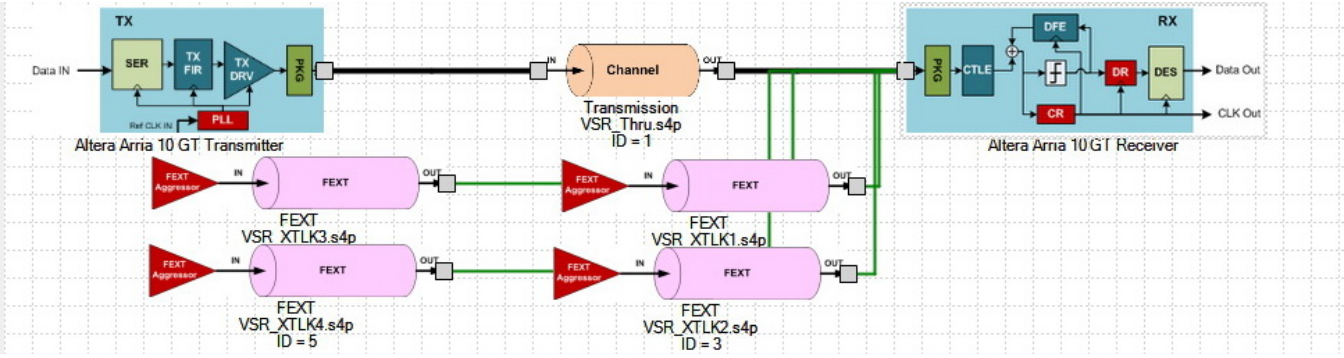
This tutorial uses JNEye to run an OIF VSR 28 Gbps link simulation using Altera's Arria 10 GT devices. The link topology is shown in the following figure.

Note: This link configuration and simulation are for demonstration purposes. It is not intended for actual implementation. Consult Altera design guidelines for actual high-speed link design and implementation.

Figure 4-1: Example OIF VSR 28G Link Topology



Methodology

This simulation emulates an Altera Arria 10 GT transmitter (with embedded package model), an OIF 25 Gbps VSR channel (with crosstalk), and an Altera Arria 10 GT receiver (with embedded package model). The link operates at 28 Gbps with a transmitter differential output voltage (V_{OD}) of about 1000 mV. The test pattern is PRBS-31 and the BER target is 10^{-15}. Per Arria 10 GT specifications, the transmitter has a 5-tap FIR and the receiver has CTLE and a 1-rap DFE (at 28 Gbps). DFE is not required in the OIF VSR standard, so DFE is disabled in this tutorial.

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To accomplish these goals, set up a transmitter model, a receiver model, and a link with the following parameters:

- Data rate: 28 Gbps
- Test pattern: PRBS-31
- BER target: BER < 10^{-15}
- Arria 10 GT transmitter
  - V_{OD}: 28 (~1000 mV)
  - Edge rate: Per Arria 10 GT characteristics
  - 5-Tap TX-FIR (2 pre-taps and 2 post-taps)
  - Arria 10 GT package model (embedded)
  - PLL: ATX (LC) set to low bandwidth
  - Output Jitter (DCD, BUJ, and RJ are from JNEye Characterization Data Access):
    - DCD: 0.015 UI
    - BUJ: 0.037 UI
    - RJ: 0.211 ps_{RMS}
- Arria 10 GT receiver
  - CTLE in High Data Rate mode, Peak Frequency 3
  - DFE is disabled
  - VGA: Bandwidth 3
  - Arria 10 GT package model (embedded)
  - CDR: Bandwidth High
  - Jitter (from JNEye Characterization Data Access):
    - DJ: 0.112 UI
    - RJ: 0.421 ps_{RMS}

Figure 4-2: OIF VSR Channel Characteristics

The JNEye Channel Viewer shows that the channel has approximately 7.4 dB loss at 14 GHz. The four crosstalk channels have an amplitude of about –45 dB at 14 GHz.

Use the ideal transmitter reference clock to simulate a more ideal case. The PLL in the Arria 10 GT transmitter is enabled using ATX (LC) with low bandwidth configuration.

Use the JNEye's link optimization algorithm to find optimal equalization settings for both the transmitter and receiver. This demonstration uses the **FIR => CTLE => DFE** link optimization method.

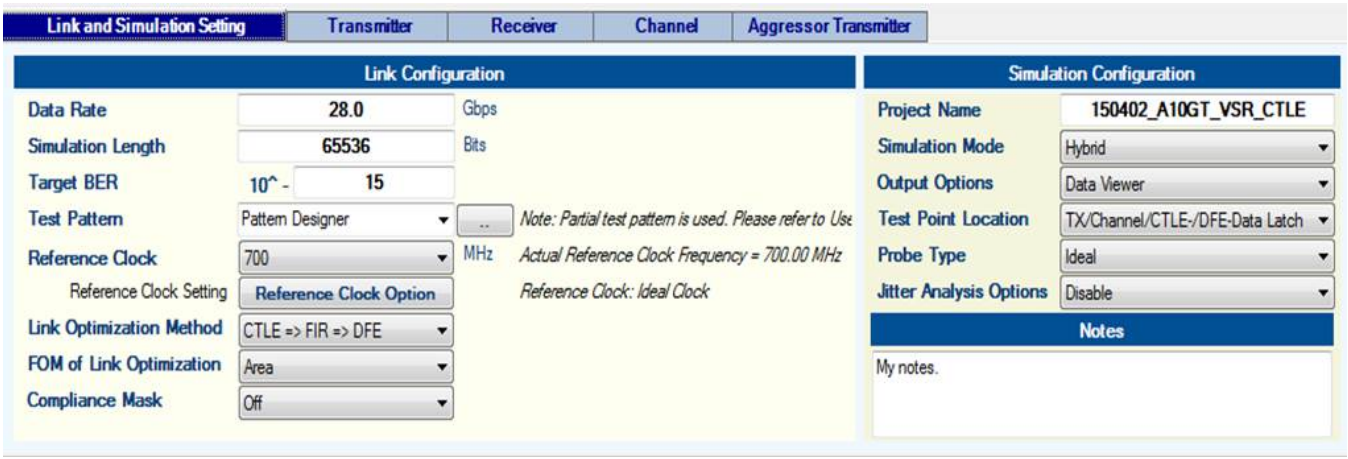
Setup and Initialization

First, start JNEye. Input the following settings in the control module.

Setting Up the Control Module

Link and Simulation Tab

Figure 4-3: Link and Simulation Settings

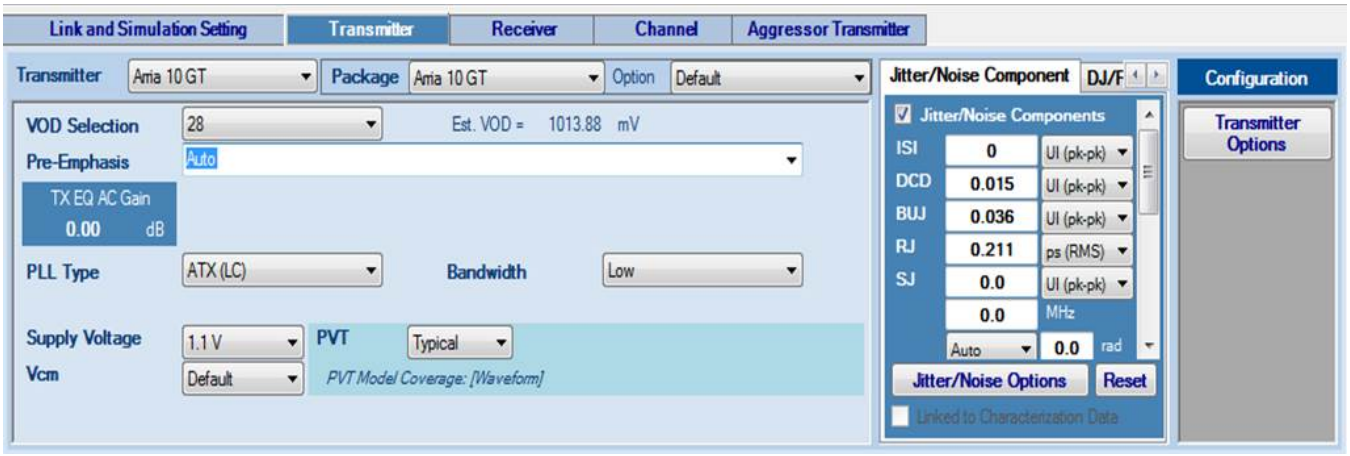


Set the following parameters in the Link and Simulation Settings tab:

- Data Rate: **28** (Gbps)
- Simulation Length: **65536** (Bits)
- Target BER: 10^ -**15**
- Test Pattern: **PRBS-31**
- Reference Clock: **700** (MHz)
- Link Optimization Method: **CTLE => FIR => DFE**
- FOM of Link Optimization: **Area**
- Compliance Mask: **Off**
- Simulation Mode: **Hybrid**
- Output Options: **Data Viewer with Image Output**

Transmitter Tab

Figure 4-4: Transmitter Settings

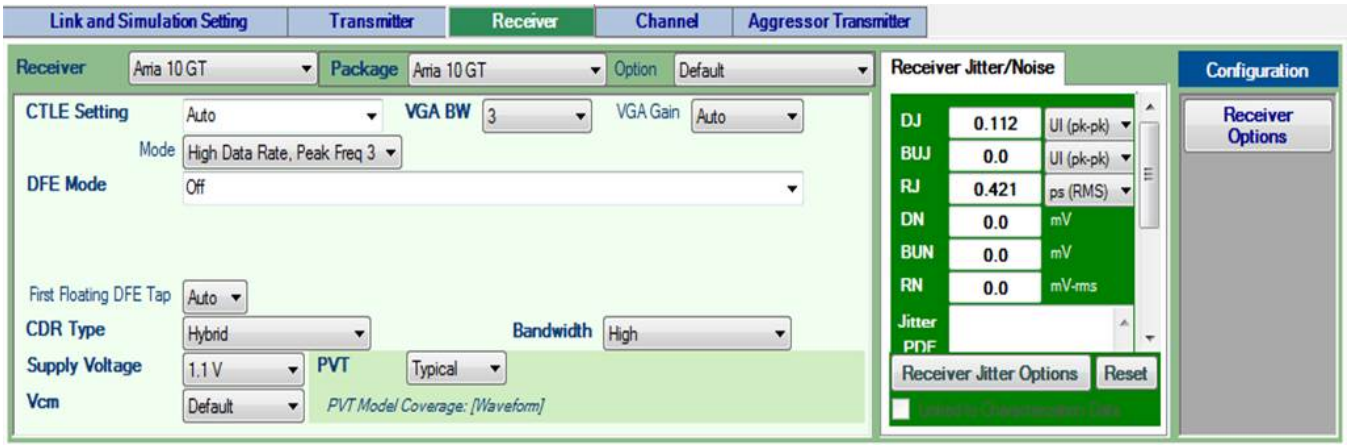


Set the following parameters in the Transmitter tab:

- Transmitter: **Arria 10 GT** (use the Link Designer or Transmitter tab to add or select a transmitter)
- Package: **Arria 10 GT**
- VOD Selection: **28** (~1000 mV)
- Pre-emphasis: **Auto**
- PLL Type: **ATX (LC)**
- PLL Bandwidth: **Low**
- Jitter/Noise Component—Retrieve the Arria 10 GT transmitter intrinsic jitter values from JNEye's Characterization Data Access by clicking **Characterization Data Access**. This populates Arria 10 GT's DCD, BUJ, and RJ values. The final TX jitter configuration is:
  - DCD: **0.015** UI in **Clock DCD** type
  - BUJ: **0.036** UI in **Uniform** distribution
  - RJ: **0.211** ps_{RMS}

Receiver Tab

Figure 4-5: Receiver Settings



Set the following parameters in the Receiver tab:

- Receiver: **Arria 10 GT** (use the Link Designer or Receiver tab to add or select a receiver)
- Package: **Arria 10 GT**
- CTLE Setting: **Auto**
- CTLE Mode: **High Data Rate, Peak Freq 3**
- VGA BW: **3**
- VGA Gain: **Auto**
- DFE Mode: **Off**
- CDR Type: **Hybrid**
- CDR Bandwidth: **High**
- Jitter/Noise Component—Retrieve the Arria 10 GT receiver intrinsic jitter values from JNEye's Characterization Data Access by clicking **Characterization Data Access**. This populates Arria 10 GT's DJ and RJ values. The jitter value and jitter properties are linked to JNEye's embedded characterization database, which is automatically adjusted when the link or device configuration changes. The receiver jitter configuration is:
  - DJ **0.112** UI
  - RJ: **0.421** ps_{RMS}

Constructing the Channel

Next, construct the channel between the transmitter and receiver. In JNEye, the package models for the Arria 10 GT transmitter and Arria 10 GT receiver are embedded. The transmitter and receiver packages are automatically included in the simulation.

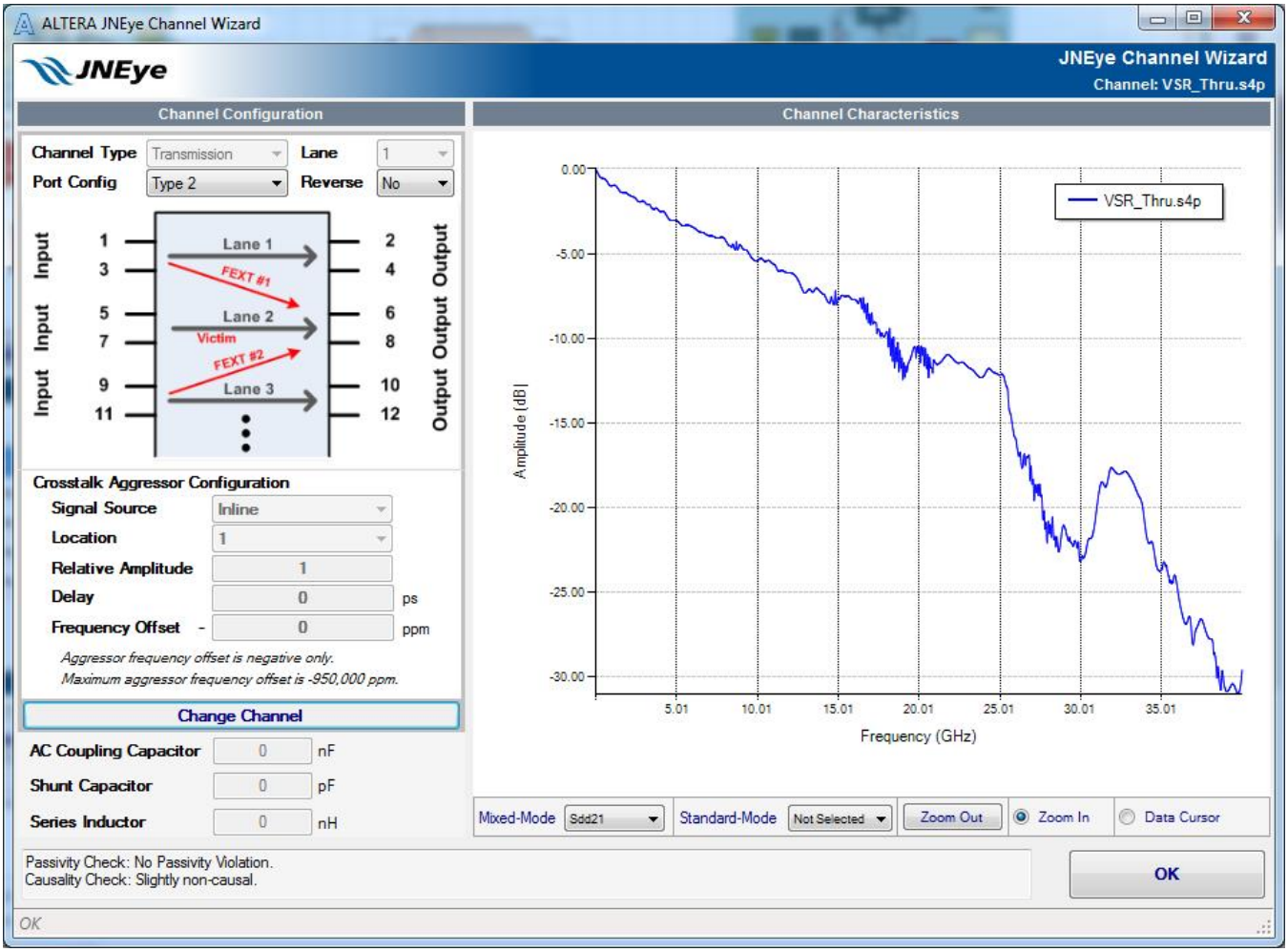
JNEye supports **crosstalk modeling** capabilities. The channel engine and simulation engine can extract and interpret crosstalk characteristics from a single or a multi-lane S-parameter file and compute the crosstalk effects. In the channel list, crosstalk channels are assumed to run in parallel with the victim channel and the crosstalk noises are superimposed. This section describes how to set up crosstalk simulation in JNEye.

The backplane model is provided as five 4-port S-parameters. It consists of one insertion loss (victim) model and four crosstalk models. Therefore, you are going to insert five channels one at a time.

Perform the following steps to add a victim channel:

1. Click **Channel** in the Link Designer and select **Transmission**.
2. Use the file browser to locate the channel model file **VSR_Thru.s4p** and add it to the channel list as victim.
3. The JNEye Channel Wizard displays the S_{dd21} characteristics. JNEye automatically detected the port configuration of this S-parameter (Type 2 in this case).
4. Click **OK** to close the Channel Wizard.
5. Place the channel icon in the Link Designer.

Figure 4-6: Configure Victim Channel with JNEye Channel Wizard



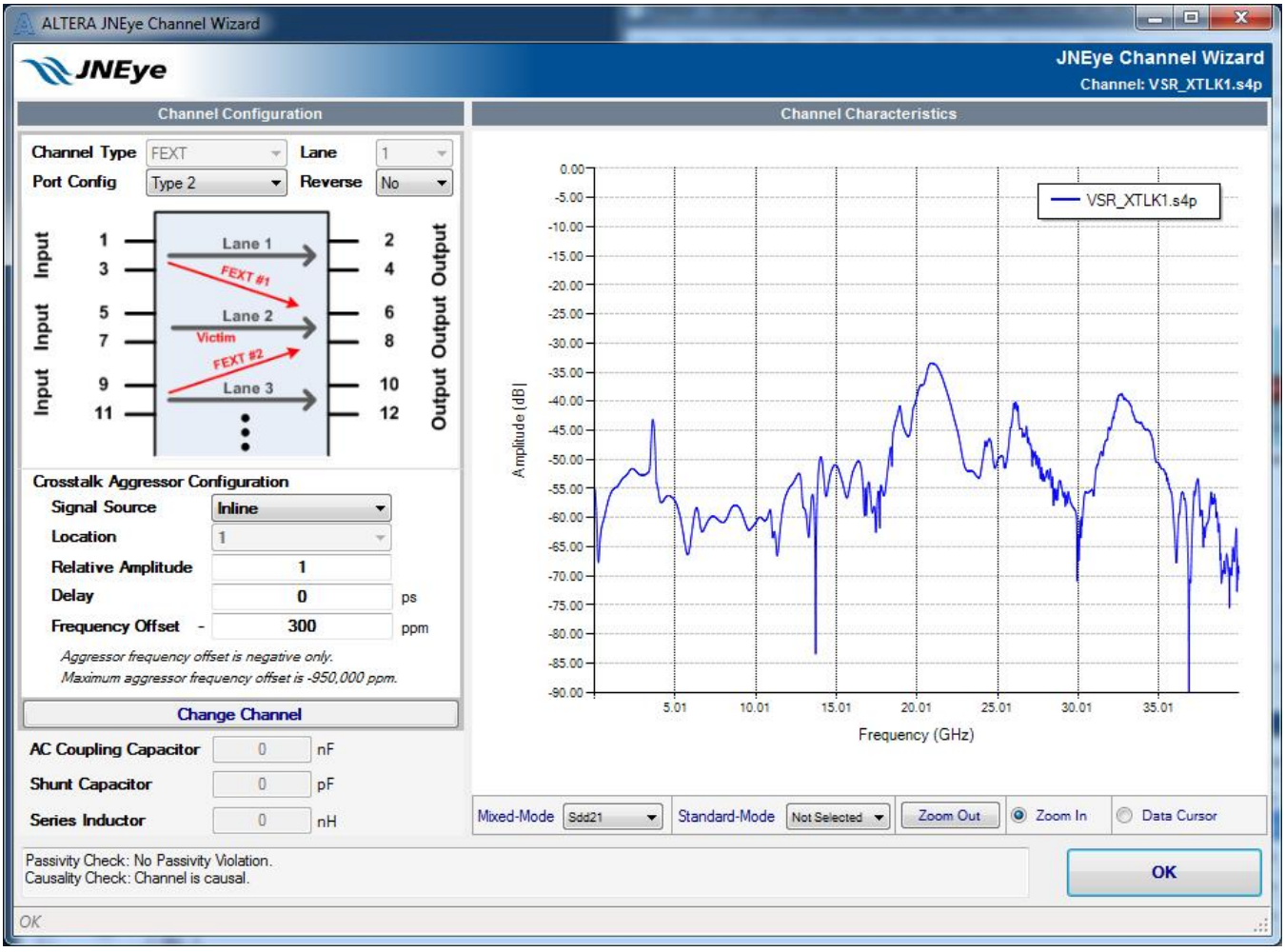
Perform the following steps to add the first crosstalk channel:

1. Click **Channel** in the Link Designer panel and select **Far-end Crosstalk (FEXT)**.
2. Use the file browser to locate the channel model file **VSR_XTLK1.s4p** and add it to the channel list as FEXT.

- Because the crosstalk channel is provided as a single-lane 4-port S-parameter, there is no difference between near-end (NEXT) and far-end (FEXT) crosstalk. Choosing NEXT or FEXT yields the same result.
- Check and validate the port configuration of crosstalk channels. Because non-transmission channels have more diverse channel characteristics, JNEye's ASCC (Automatic S-parameter Configuration Checker) can sometimes misinterpret the channel port configuration.

3. The JNEye Channel Wizard displays the FEXT #1 characteristic. Because the crosstalk is provided as single-lane 4-port S-parameter, the aggressor location selection is ignored.
4. Set the frequency offset to **300** ppm to introduce phase-shifting effect to this crosstalk noise source. This indicates the aggressor will not be frequency synchronous to the victim channel.
5. Click **OK** to close the Channel Wizard.
6. Place the channel icon in the Link Designer.

Figure 4-7: First Far-end Crosstalk Configuration in Channel Wizard

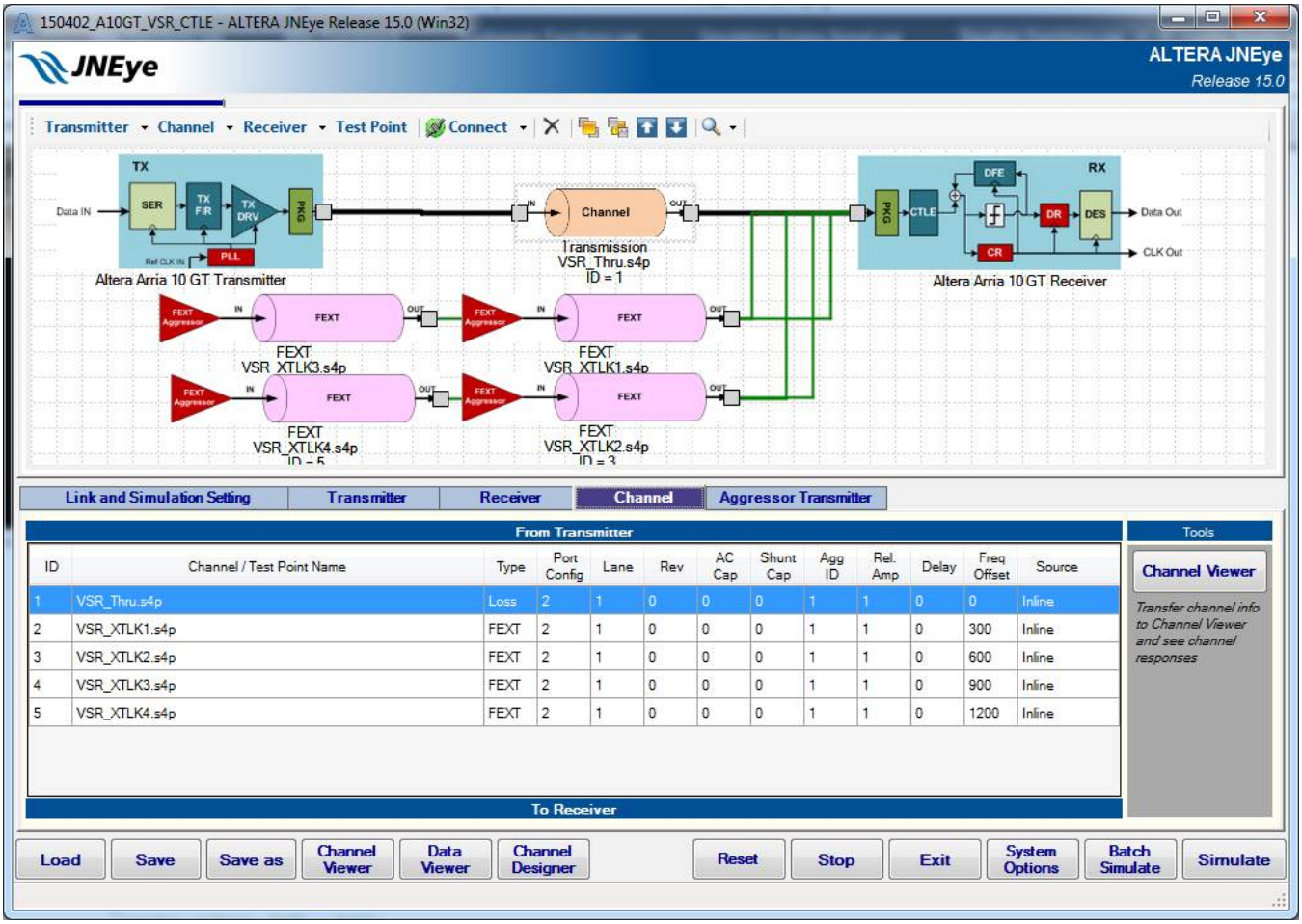


7. Add three more crosstalk channels using this procedure. Add the channel model files **VSR_XTLK2.s4p**, **VSR_XTLK3.s4p**, and **VSR_XTLK4.s4p** to the Link Designer workspace. Assign the following frequency offsets for each crosstalk channel, respectively: **600** ppm, **900** ppm, and **1200** ppm.

Completing the System

All the link components are now chosen and placed in the Link Designer. Click **Connect** in the Link Designer to begin connecting the components. Refer to the *Link and Simulation Setting* section for link construction in the Link Designer. The following figure shows the completed link system.

Figure 4-8: Complete VSR 28 Gbps Link Connection in Link Designer



The link configuration is complete. Use the **Save/Save as** buttons to save the configuration for later use.

Analysis

Use the **Channel Viewer** to observe and analyze the channel characteristics. The **Channel Viewer** button is located on the right side of the Channel tab. This example shows the S_{dd21} of the five channels you selected as well as the channel responses at test points and the overall channel. You can leave the **Channel Viewer** module open or close it by clicking **OK** or **Exit**.

Figure 4-9: Channel Characteristics of Victim and 2 FEXT Channels

Start the channel simulation by clicking **Simulate** in the lower right corner of the JNEye Control Module. The JNEye Simulation Engine excises all the models and generates eye diagrams at test points and inside the receiver (after CTLE and DFE).

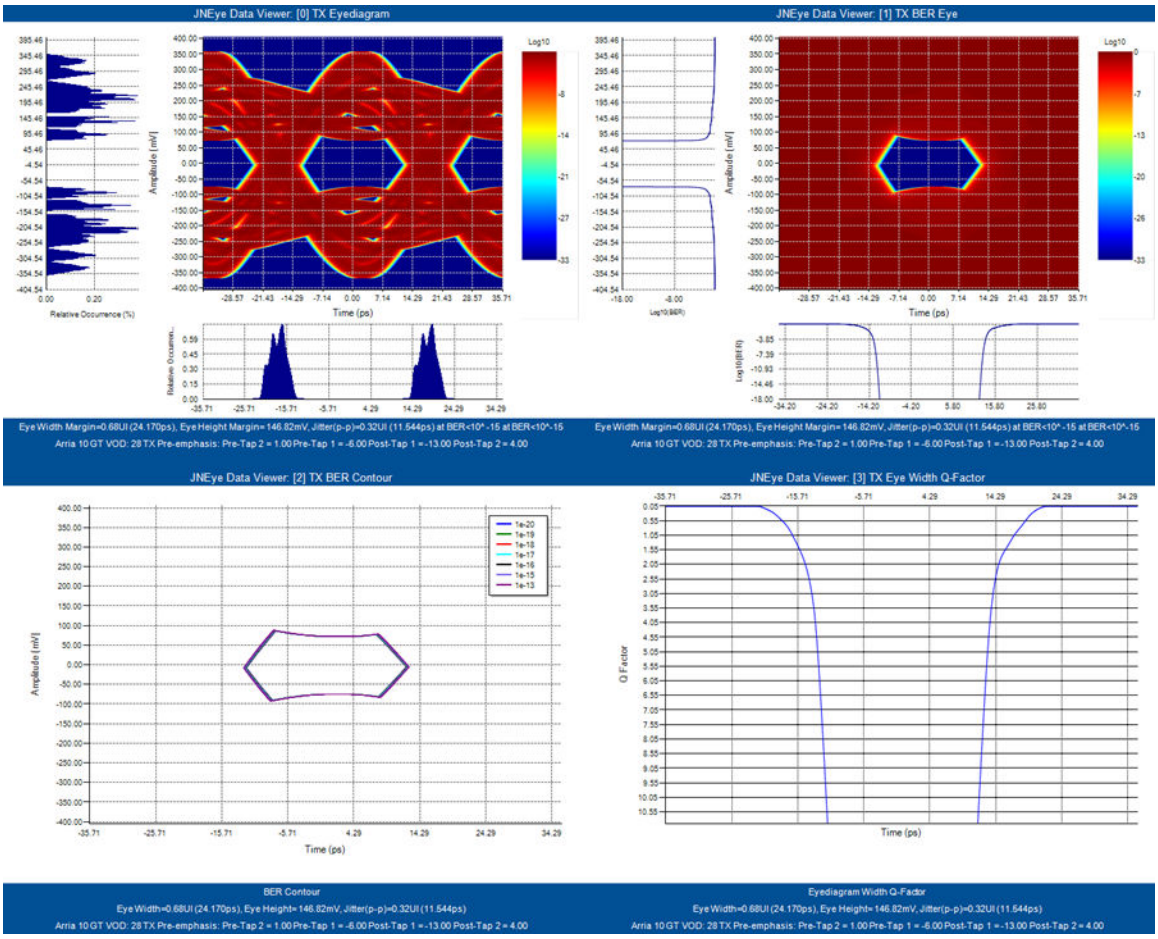
A goal of this tutorial was for JNEye to automatically find the optimal link setting for both transmitter and receiver. In the simulation time, the progress bar flashes multiple times, indicating the JNEye Simulation Engine is exploring the solution space. The link performance and result of the final setting is shown in a JNEye Data View.

At TX output, which is located after the Altera Arria 10 GT transmitter output pin (after the TX package model), the results are shown in the following figure. JNEye found the optimal TX-FIR setting: **Pre-tap 2 = 1**, **Pre-tap 1 = –6**, **Post-Tap 1 = –13**, and **Post-Tap 2 = 4**. The configured transmitter generates ~0.32 UI of jitter at BER = 10^{-15}. This set of TX outputs is measured with the transmitter's intrinsic jitter and additional sinusoidal jitter using the ideal clock reference.

- The first figure (top left) is a hybrid eye diagram that includes deterministic jitter and probability density function (PDF) because of unbounded jitter and noise sources.
- The second figure (top right) contains the cumulative distribution (CDF) eye diagram with BER bathtub curves (for both width and height in the eye diagram opening).
- The third plot (lower left) is a BER contour plot that shows the eye diagram opening area at various BER targets.
- The fourth plot shows Q-Factor curves, which are another representation of BER bathtub curve using Q-factor by assuming the noise/jitter is Gaussian.

With the Gaussian random jitter injected into the link, the BER bathtub and Q-Factor plots clearly show the effects where this unbounded jitter narrows the eye diagram width as the BER target reduces.

Figure 4-10: TP1 Hybrid Eye Diagrams and BER Analysis Measured with Ideal Clock

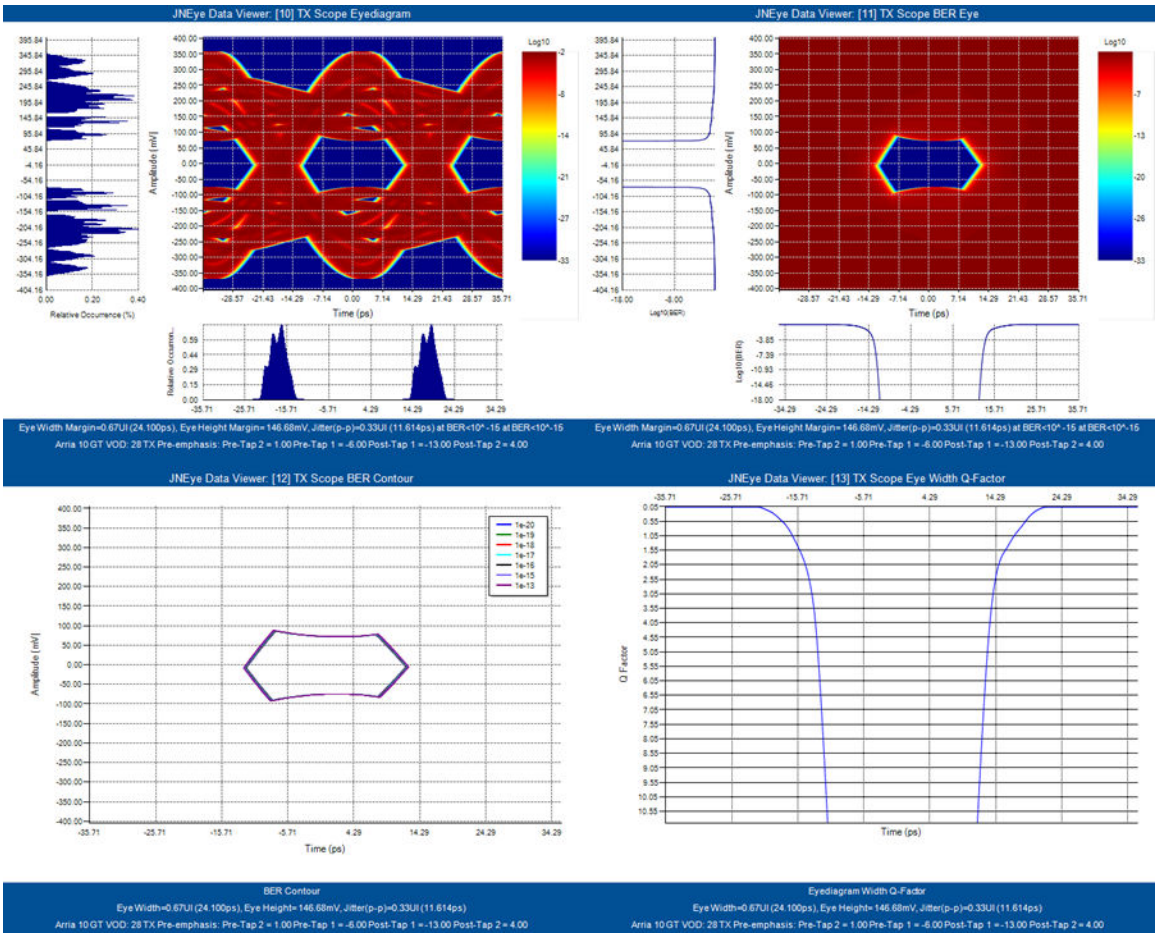

JNEye Data Viewer: [0] TX Eyediagram
JNEye Data Viewer: [1] TX BER Eye
JNEye Data Viewer: [2] TX BER Contour
JNEye Data Viewer: [3] TX Eye Width Q-Factor
Time (ps)
Amplitude [mV]
Q Factor
BER Contour
Eyediagram Width Q-Factor

The second set of TX outputs are measured with the golden CDR, which has a loop bandwidth of 1/1667 of the data rate. This set of outputs reflects the common lab scope measurement. With the golden CDR in place, the low frequency jitter (such as the 1 MHz sinusoidal jitter) and noise, which are included in phase noise and spurs, are tracked.

When you enable a PLL in a transmitter, the reference clock's phase noise is shaped and filtered with the PLL's response. For a demonstration of PLL and transmitter reference clock phase noise, refer to the *JNEye Tutorial: PCI Express 8GT*.

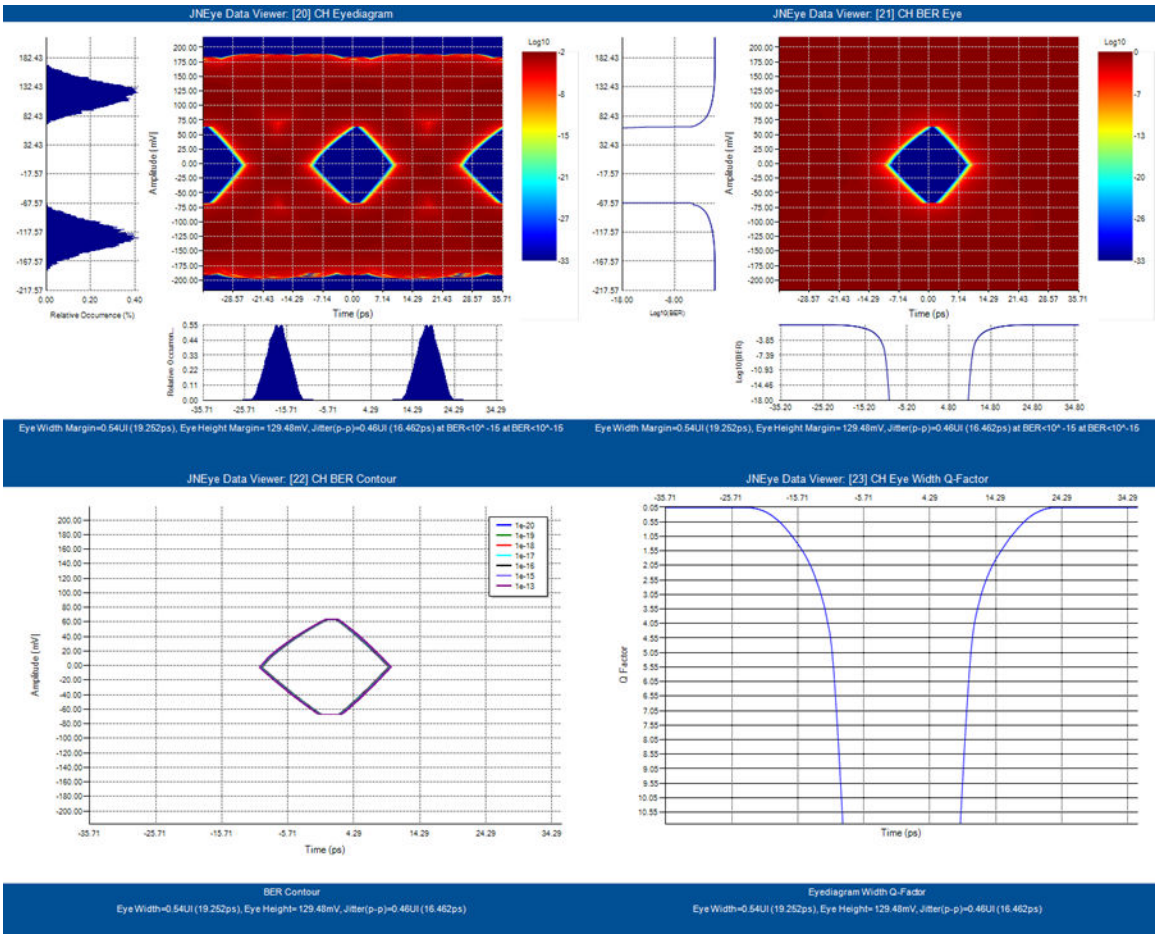
The following figure shows that the transmitter output jitter, which includes the transmitter output jitter, is about 0.33 UI at BER 10^{-15}.

Figure 4-11: Transmitter Scope Output Measured with Golden CDR


JNEye Data Viewer: [10] TX Scope Eyediagram
JNEye Data Viewer: [11] TX Scope BER Eye
JNEye Data Viewer: [12] TX Scope BER Contour
JNEye Data Viewer: [13] TX Scope Eye Width Q-Factor
Time (ps)
Amplitude (mV)
Q Factor
BER Contour
Eyediagram Width Q-Factor

At the channel output, which is located at the end of the OIF VSR channel with crosstalk, the opening eye area is reduced because of the channel loss, crosstalk, and input jitter from TX and additional sinusoidal jitter. The eye diagram opening is about 0.54 UI and 1.29 mV at BER = 10^{-15}.

Figure 4-12: Channel Output Hybrid Eye Diagrams and BER Analysis


JNEye Data Viewer: [20] CH Eyediagram
JNEye Data Viewer: [21] CH BER Eye
Eye Width Margin=0.54UI (19.252ps), Eye Height Margin= 129.48mV, Jitter(p-p)=0.46UI (16.462ps) at BER<10^-15 at BER<10^-15
Eye Width Margin=0.54UI (19.252ps), Eye Height Margin= 129.48mV, Jitter(p-p)=0.46UI (16.462ps) at BER<10^-15 at BER<10^-15
JNEye Data Viewer: [22] CH BER Contour
JNEye Data Viewer: [23] CH Eye Width Q-Factor
Amplitude [mV]
Time (ps)
Relative Occurance (%)
Log10(BER)
Q Factor
BER Contour
Eye Width=0.54UI (19.252ps), Eye Height= 129.48mV, Jitter(p-p)=0.46UI (16.462ps)
Eyediagram Width Q-Factor
Eye Width=0.54UI (19.252ps), Eye Height= 129.48mV, Jitter(p-p)=0.46UI (16.462ps)

At the CTLE output, the signal after the receiver's CTLE, the Arria 10 GT CTLE AC gain level 13 is identified by JNEye's link optimization algorithm as the optimal CTLE setting. Similar to the TX output case, when the receiver CDR is enabled or included in the simulation, two sets of CTLE outputs are shown. The first set of outputs is with the ideal clock and the second one is with the CDR recovered clock. The total jitter is 0.69 UI (at BER < 10^{-15}, with ideal clock) or 0.67 UI (with CDR recovered clock, if DFE is not used). The eye diagram opening height margin is 83 mV (at BER < 10^{-15}, with ideal clock) and 90 mV (with recovered clock). Because both the transmitter and receiver intrinsic jitter are included in the simulation, the eye opening indicates the link margin at this observation point. Note that the eye opening is smaller than the channel output results because the receiver intrinsic jitter is included in the CTLE output results.

When you enable the CDR in a receiver, the transmitter random jitter is shaped and filtered with the CDR's response. Refer to the *JNEye Tutorial: PCI Express 8GT* for a demonstration of this part.

Figure 4-13: CTLE Output Hybrid Eye Diagram and BER Analysis with Ideal Clock

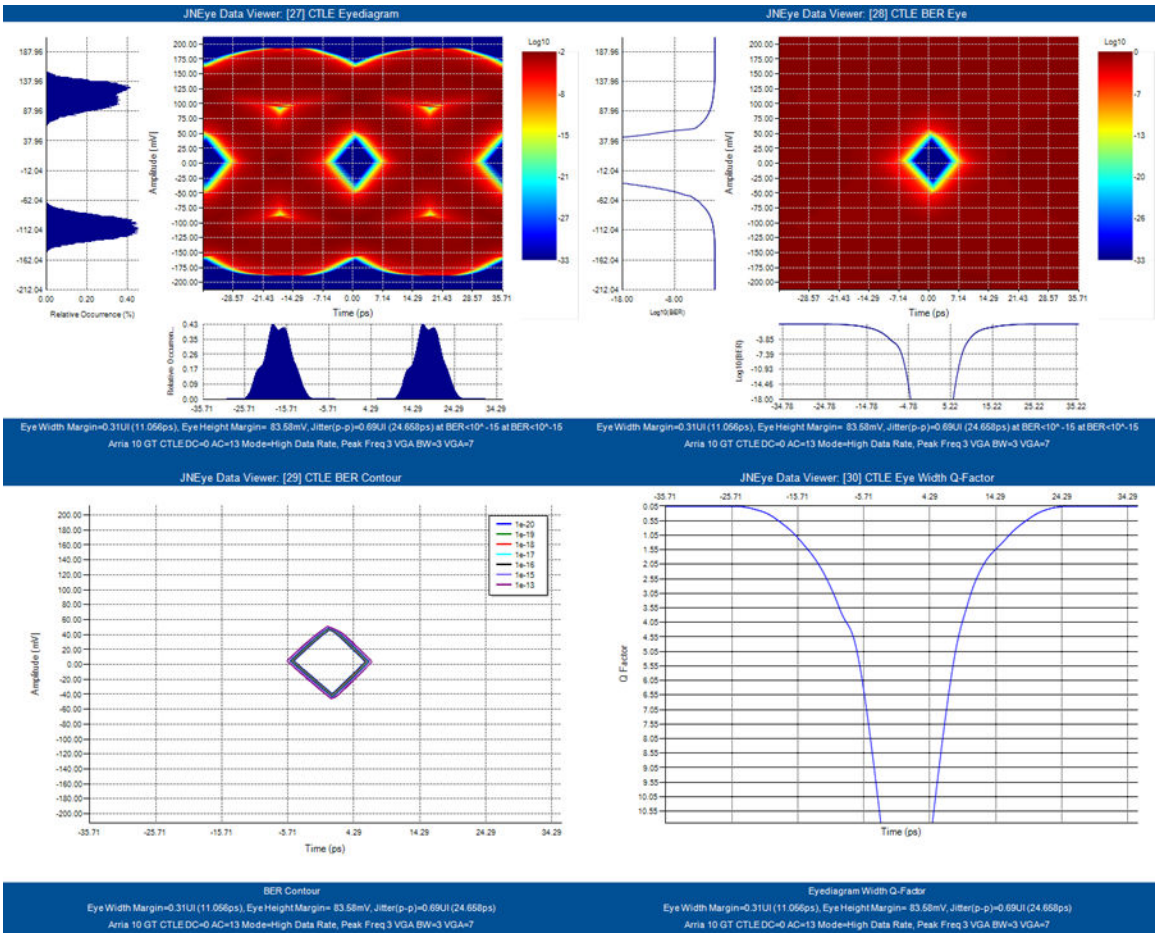
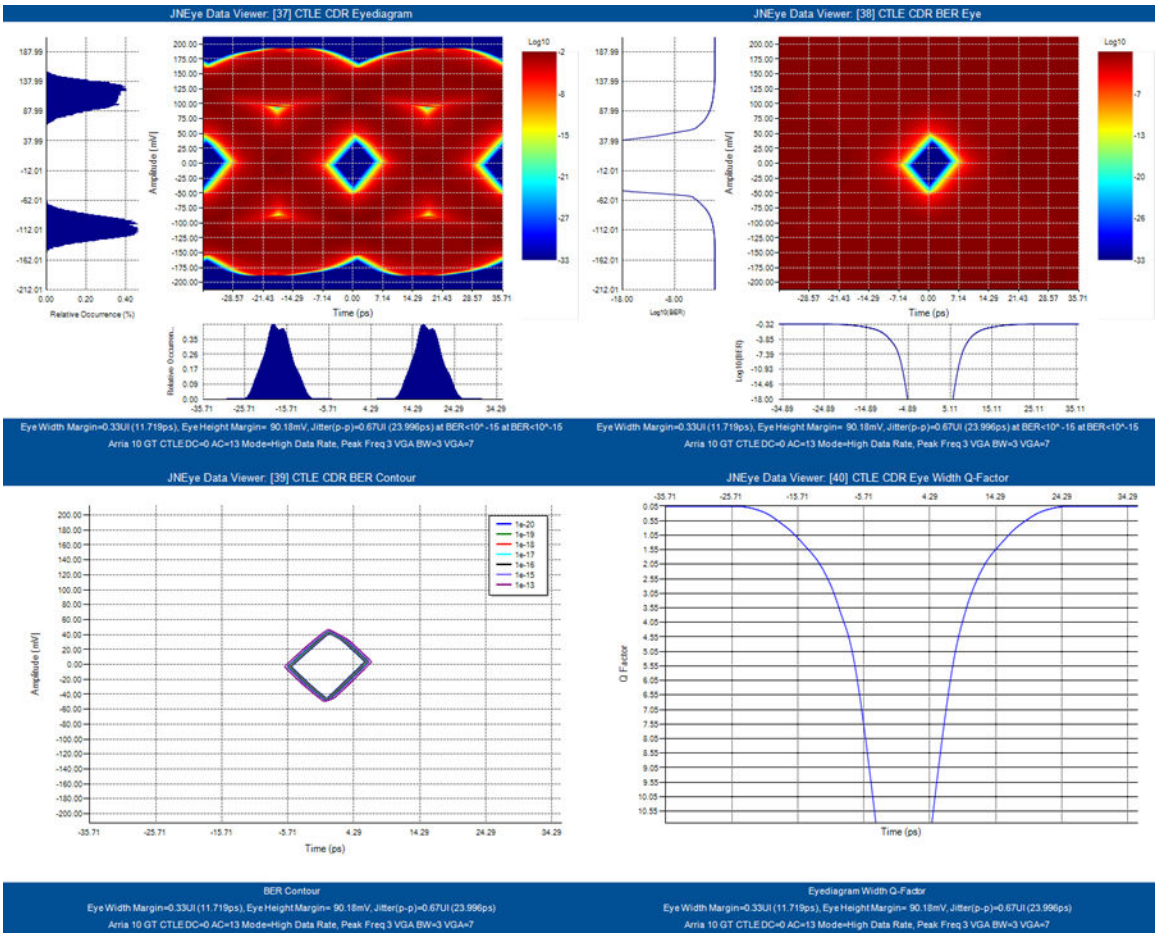

JNEye Data Viewer: [27] CTLE Eyediagram
JNEye Data Viewer: [28] CTLE BER Eye
Eye Width Margin=0.31UI (11.066ps), Eye Height Margin= 83.58mV, Jitter(p-p)=0.69UI (24.668ps) at BER<10^-15 at BER<10^-15
Arria 10 GT CTLE DC=0 AC=13 Mode=High Data Rate, Peak Freq 3 VGA BW=3 VGA=7
JNEye Data Viewer: [29] CTLE BER Contour
JNEye Data Viewer: [30] CTLE Eye Width Q-Factor
Time (ps)
BER Contour
Eyediagram Width Q-Factor

Figure 4-14: CTLE Output Hybrid Eye Diagram and BER Analysis with CDR Recovered Clock


JNEye Data Viewer: [37] CTLE CDR Eyediagram
JNEye Data Viewer: [38] CTLE CDR BER Eye
JNEye Data Viewer: [39] CTLE CDR BER Contour
JNEye Data Viewer: [40] CTLE CDR Eye Width Q-Factor
Time (ps)
Amplitude (mV)
Q Factor
BER Contour
Eyediagram Width Q-Factor

This example demonstrated how to use JNEye to set up an OIF VSR 28 Gbps serial link with Altera's Arria 10 GT devices and evaluate its link performance. JNEye allows you to:

- Configure a link
- Configure an external reference clock
- Configure a transmitter and receiver
- Configure a channel
- Configure and model jitter and noise sources
- Derive accurate jitter figures for Altera devices from the Altera JBE database
- Load and save a link configuration
- Observe the channel characteristics
- Set up test points within the link
- Compute and observe an eye diagram
- Perform BER analysis

Additional Information 5

2015.05.04

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Additional information about the document and Altera.

Document Revision History

Date	Version	Changes
May 2015	2015.05.04	• Updated channel compliance check and analysis documentation in the *JNEye Channel Viewer* section. • Updated the PCI-Express tutorial with new measurements and results. • Updated the OIF VSR tutorial with new configuration and results. • Updated most GUI screenshots to reflect 15.0 changes.
December 2014	2014.12.15	• Added the *JNEye Channel Designer* section. • Added channel compliance check and analysis documentation in the *JNEye Channel Viewer* section. • Updated the two tutorials with new measurements and results. • Updated all GUI screenshots with new plots.
June 2014	2014.06.30	• Incorporated new features of the JNEye Channel Viewer. • Added new waveform display feature. • Updated the Arria 10 models. • Updated all GUI screenshots with new plots.
December 2013	2013.12.09	Initial release.

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